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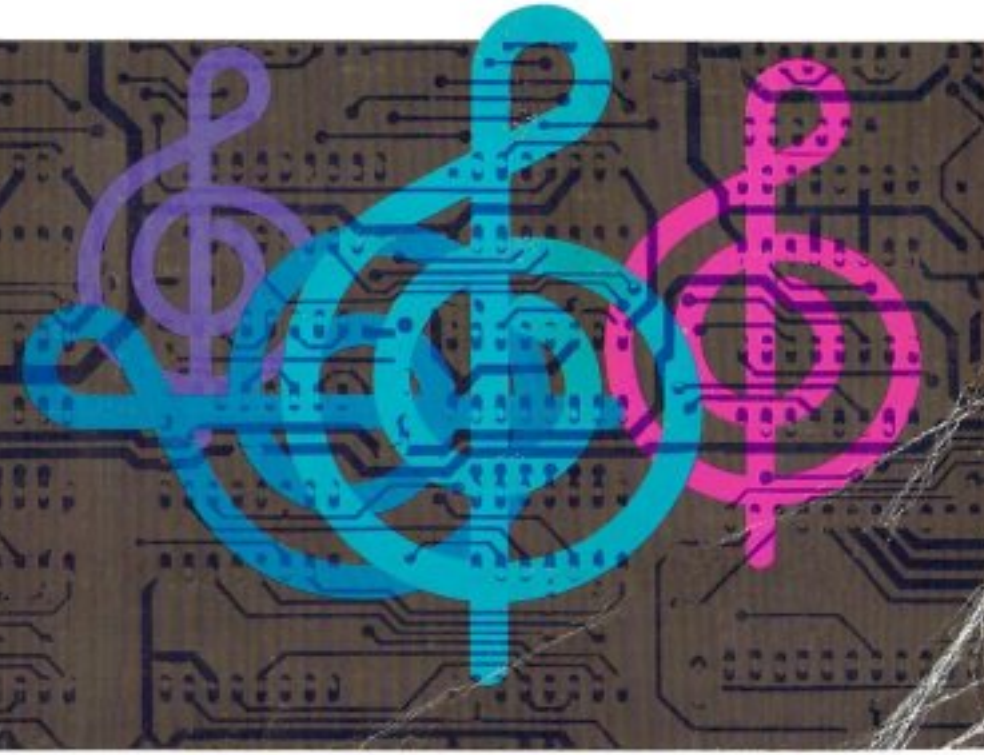
# ELECTRONIC MUSIC CIRCUITS

BY BARRY KLEIN



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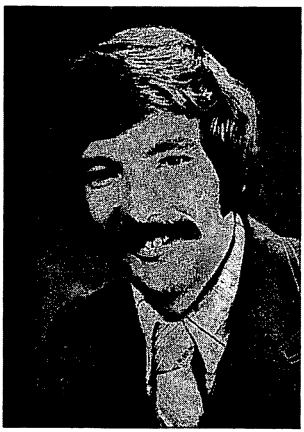
# Electronic Music Circuits



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# Electronic Music Circuits

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# PREFACE

The field of electronic music is undergoing an electronics revolution similar to the current microprocessor/microcomputer revolution. Initially music synthesizers were built using discrete components—transistors, resistors, capacitors, etc. Synthesizer modules were fairly complex in design and were subject to temperature stability and reliability problems due to the large number of individual components used. With the integrated circuit (IC) revolution of the early seventies, designs became more reliable and the parts count was reduced. Soon hobbyists and manufacturers were producing impressive synthesizer systems and the synthesizer became an important instrument for today's music.

During the last few years a number of common elements in synthesizer design have been refined and put in single IC form. Currently there are voltage controlled oscillators, amplifiers, filters, envelope generators, multipliers, and noise sources available in single IC form. Using these devices it is fairly easy to develop a patch-panel (modular) synthesizer system in which an indefinite number of effects can be created.

In Chapter 1 some basic sound and synthesizer characteristics are discussed, along with some of the typical signal level and control voltage specifications. In Chapter 2 basic power supplies are explained, along with a number of designs that can be used in a synthesizer. Keyboards are covered in Chapter 3 and different types of controllers and control voltage generators, such as joysticks, pressure-sensitive controllers, envelope generators, and ribbon controllers are discussed.

Voltage controlled oscillators are an extremely important synthesizer building block, and they are dealt with in Chapter 4. These devices generate one or more signal or control waveforms (triangle, sawtooth, sine, pulse, etc.) and are used with many of the other building blocks in a synthesizer.

The next chapter covers various types of filters used in synthesizer systems, including the many varieties of voltage controlled filters and the graphic equalizer. These devices can be designed using standard op amps or using some of the sophisticated filter chips that are now available.

In Chapter 6 analog multipliers are discussed, based on both discrete and integrated circuit designs. Examples of analog multipliers include the voltage controlled amplifier and the four-quadrant multiplier. These devices are useful for amplitude control and signal modulation effects.

Chapter 7 is a collection of several different circuits, including analog delay circuits and timbre modulators. In Chapter 8 the design of a basic modular system including signal input and output requirements is described.

This book takes the reader through the design of the various components that make up an electronic synthesizer, up to the point of designing a system and assembling it. At that point the reader's imagination must take over, because an unlimited number of effects and sounds can be produced.

BARRY KLEIN

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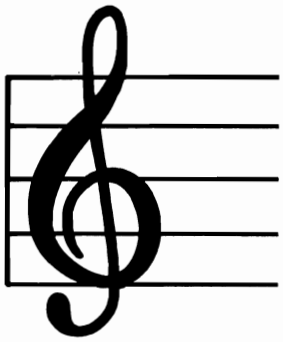
# SYNTHESIZER SYSTEM DESIGN



# CHAPTER 1

An electronic music snythesizer is a system of *signal generation* and *modification* circuits wired together to enable a person to obtain sounds of a predictable and/or musical quality. The secret of the synthesizer's success is its versatility. The synthesizer (see Fig. 1–1) provides almost total control over the parameters of the sound.

## THE PARAMETERS OF SOUND

The three basic characteristics of a sound are its *pitch*, its *dynamics*, and its *tonal character*, or *timbre*.

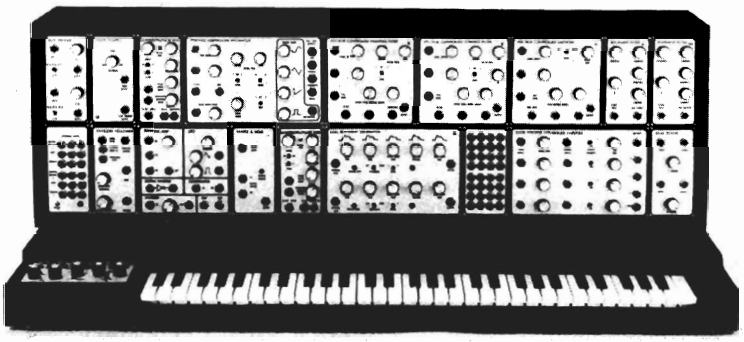


**Fig. 1-1. A modular analog synthesizer.** *(Courtesy E-mu Systems)*

## Pitch

The *pitch* of a sound is perceived in the listener's mind—not read on a meter. Pitch is often thought to be the same as frequency. They are related but separate properties. *Frequency* is the measurement of a waveform's repetition rate. Frequency is measured in cycles per second, or *hertz* (Fig. 1–2). One-thousand hertz is called one *kilohertz*.

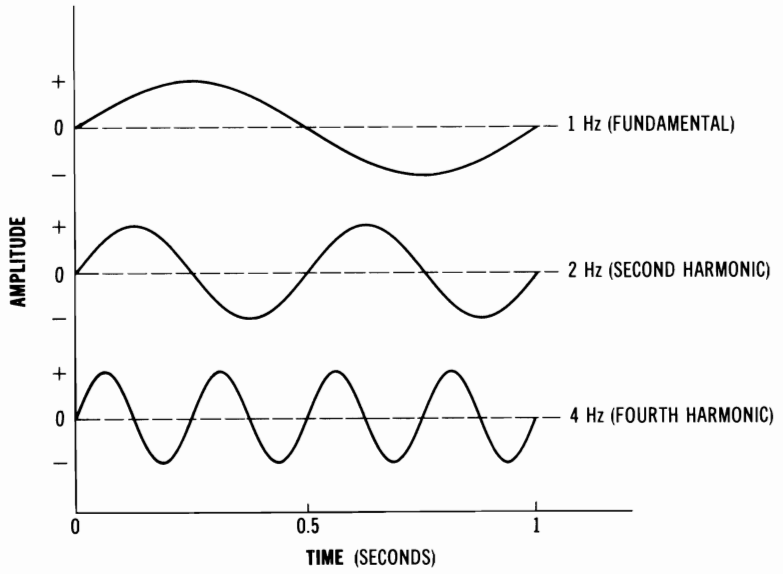



**Fig. 1-2. Harmonically related sine waves.**

Although the sound *waveform* has a frequency that can be measured by a frequency meter, unless it is a sine wave it consists of a combination of different frequencies at different amplitudes. Sometimes these frequencies are related mathematically as integral (1, 2, 3, . . . ) multiples of a single base frequency, which is called the *fundamental*. Integral multiple frequencies of the fundamental are called *harmonics* (Fig. 1–2). The *sine wave* is the only waveform that contains no harmonics (Fig. 1–3).

Often waveforms contain other frequencies that are not integral multiples of the fundamental. These frequencies are called *partials*. They often come close to being harmonics and are prevalent in most natural musical sounds.

| WAVEFORM | DESIGNATION | HARMONIC CONTENT | HARMONIC AMPLITUDE RELATIONSHIPS |
|---|---|---|---|
| | SINE | 0 | 0 |
| | SAWTOOTH | 1,2,3.... | EXPONENTIAL |
| | TRIANGLE | 1,3,5,7.... | 1/9,1/25,1/49.... |
| | SQUARE | 1,3,5,7.... | 1/3,1/5,1/7.... |

**Fig. 1-3. Typical synthesizer waveforms and their harmonic content.**

Some musical instruments, such as the pipe organ, produce a sound that consists of harmonics of a fundamental though the fundamental is not actually present in the sound waveform. The pitch of the fundamental is perceived but not actually generated. This illustrates the difference between pitch and frequency.

## Dynamics

The *dynamic*, or *amplitude*, characteristics of a sound are called the sound's *envelope*. This envelope consists of an initial *attack*, *a sustain*, and *a decay*. Fig. 1–4 shows the envelope of a plucked string on a guitar.

The initial *attack* of a guitar's envelope is quite fast and high in amplitude due to the large amount of energy stored in the string the moment before it is released from the pick. The attack of a reed instrument, however, is gradual because of the need to build up energy in the form of increasing air pressure. The *sustain* of a sound is its average steady-state volume level. The *decay* of a sound is its dying out caused by a loss of energy. In a guitar this would be due to insufficient resonant feedback from its body or amplifier.

## Timbre

Finally, one of the most important characteristics (and hardest to duplicate) of a sound is its *tonal character*, or *timbre*. This is the character of a musical tone that distinguishes one musical instrument from another playing the same tone. It is mostly a sound's variation in frequency content (not pitch) with time. The time variable is the important characteristic to remember if

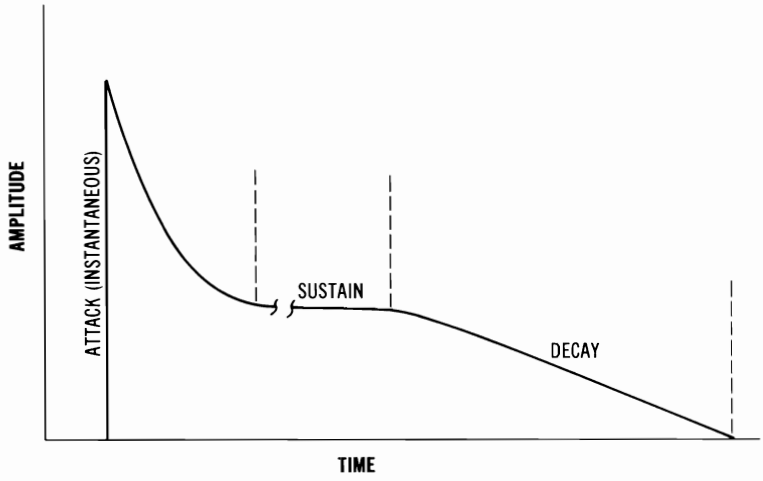



**Fig. 1-4. The envelope of a guitar.**

you wish to duplicate an instrument's timbre. You can't play a note on your instrument, take a "picture" of the sound's waveform, duplicate it with your synthesizer, and expect it to sound exactly like the instrument. The moment after you took the picture of the waveform, it changed completely in waveshape (and thus in frequency content). It is for this reason that many synthesists (synthesizer users) do not expect to duplicate an instrument's sound; rather, they try to get something close to the same *effect*. However, the closer the synthesizer's sound comes to one or more conventional instruments, the more commercially acceptable it is—it's cheaper to have a synthesizer than a violin section.

## SYNTHESIS TECHNIQUES

Several techniques are used in sound synthesis today. Choice of the technique depends on several factors. Some techniques require analysis of a known sound for frequency content and mathematical analysis for control parameters of the synthesizer. Computers are often necessary in these systems for their memory and control functions. Currently this means high cost, and some knowledge of computer programming is required of the

user. Therefore most of these systems exist in university labs and studios and not in music stores.

### Additive Synthesis

*Additive synthesis* is a method of sound generation characterized by the summation of pseudo-harmonically related sound sources (usually sine wave) with slowly varying amplitudes, frequencies, and/or phases.

Small additive systems can be made up of analog modules such as those used in subtractive systems (Fig. 1–5). Several exponential vco's (voltage controlled oscillators) would be initially set up at the desired pseudo-harmonic frequencies. In this type of vco the frequency generated by the oscillator is an exponential function of the voltage input (Fig. 1–6). All vco's share a common control voltage (CV) from the keyboard. Thus, with a change in key position on the keyboard, the pitch would change but the harmonic relationships (timbre) would remain constant. Separate voltage controlled amplifiers are placed on the outputs of the vco's. Each voltage controlled amplifier is fed its own control envelope. Then all voltage controlled amplifier outputs are summed together. The end result simulates the changing harmonic content of a natural sound.

Larger systems are designed with digital circuitry. Before such a system is constructed, a selected sound, such as middle C on the piano, is first analyzed for varying frequency content. Then digital oscillators are made to produce waveforms for each harmonic present in the analyzed sound (Fig. 1–7). The waveform consists of a large number of sequential amplitude steps. Each step is represented digitally. All of the step codes for one complete cycle of the waveform are stored in memory. The memory is scanned serially from start to finish and back again for as long as the waveform is desired. The rate at which the memory is scanned determines the frequency; the frequency equals the sample rate divided by the number of steps per cycle. Usually, though, the scanning rate is crystal controlled for stability, and, instead, the digital code (the waveform memory address) is incremented to changed frequency. Amplitude control is achieved by multiplying the digital code by another digital code stored in another "envelope" register.

The final digital code is fed to a digital-to-analog converter (dac) and low-pass filtered so that all high-frequency compo-

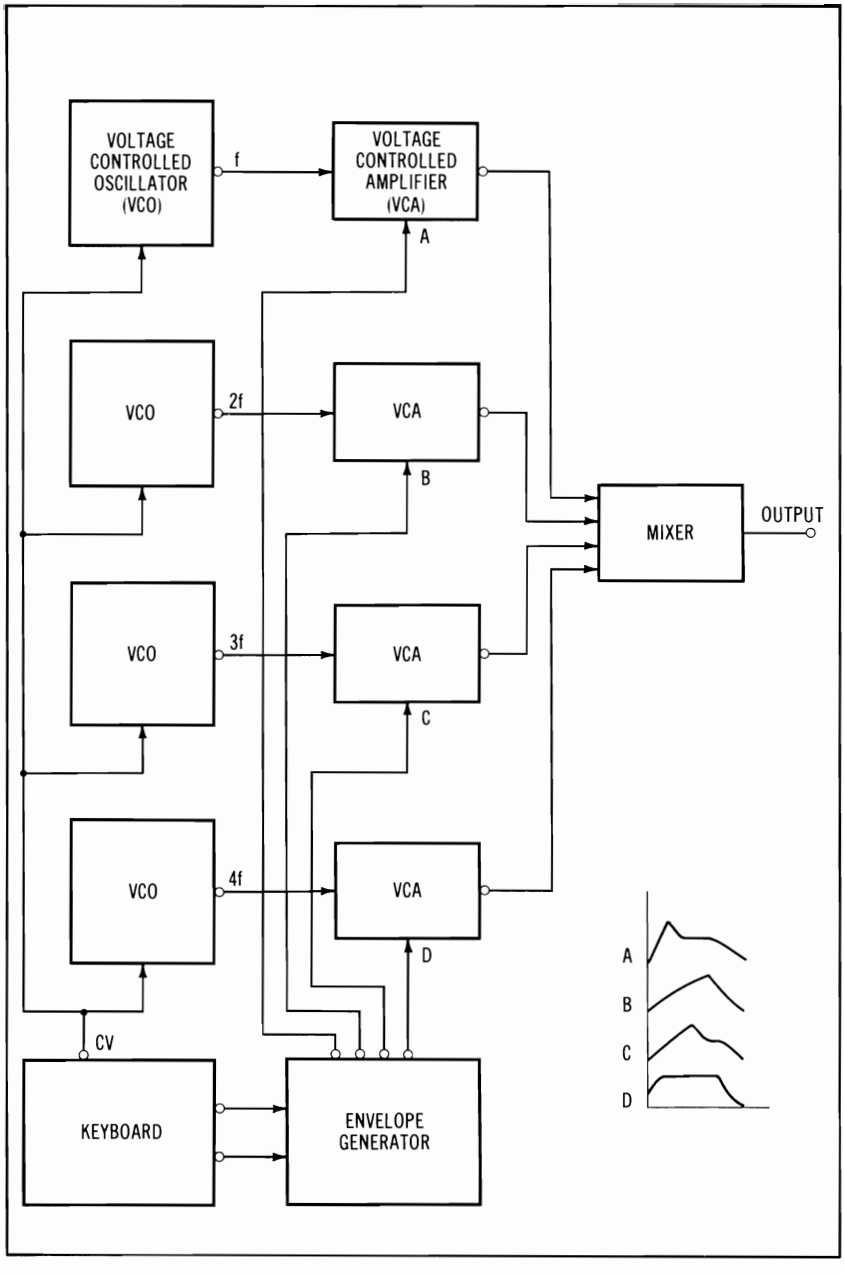



**Fig. 1-5. Additive synthesis using analog modules.**

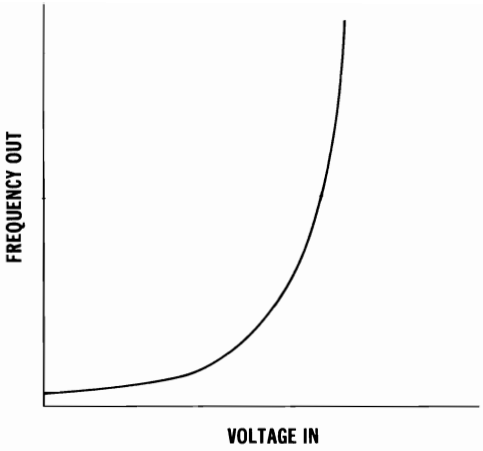



**Fig. 1-6. The voltage vs. frequency output of an exponential vco.**

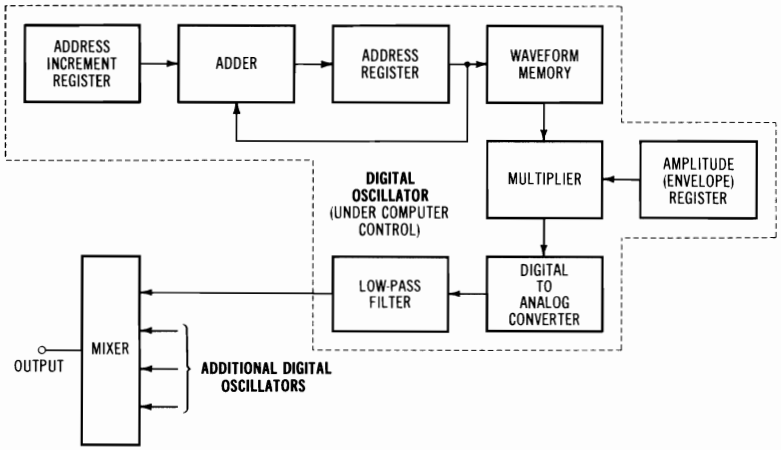



**Fig. 1-7. Additive synthesis using digital circuitry.**

nents of the sound that have frequencies above 18 or 20 kHz are removed. This waveform is then added with other similar waveforms to produce the final synthesizer output.

This method requires previous analysis of known sounds for frequency content and variation. Attempts are then made to duplicate the sound with additive techniques. The additive technique has the advantage of allowing more amplitude con-

trol over frequency content of a note with time (more natural sounds) but has the disadvantages of complexity, high cost, and great difficulty in programming in *real time*. (*Real time* means "while you are playing.") To change a parameter in the sound with a large digital additive system, a new computer program must be initiated.

### Nonlinear Synthesis

*Frequency modulation* (fm) is a *nonlinear synthesis* technique employing two oscillators, one modulating the frequency of another. The modulated oscillator output consists of frequency sidebands on either side of (and including) the original (unmodulated) frequency. The number of partials in this waveform depends on the *modulation index*, which is the ratio of frequency deviation to the frequency of the modulating wave.

Like additive synthesis, fm can be employed using analog synthesizer modules (Fig. 1–8). Many vco circuits now include linear frequency control inputs for this purpose. Frequency modulation produces sounds that are more natural sounding with less equipment.

Frequency modulation is enjoying popularity with computer music enthusiasts also. Digital oscillators are employed that are similar in design to those used in additive systems, except for the fm capability. Due to the smaller amount of circuitry needed, the computer's speed requirement is not as great. Consequently, some real-time, fm synthesis systems do exist.

Other examples of nonlinear synthesis include any methods that *distort* the original waveform in a nonlinear fashion. These may include full-wave rectification, variable clipping circuits,

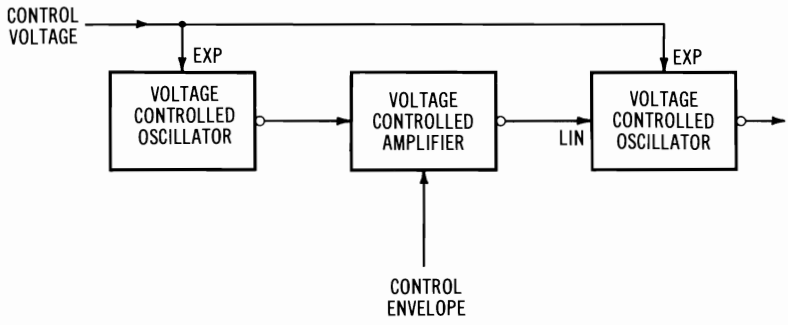



**Fig. 1-8. Fm synthesis using analog modules.**

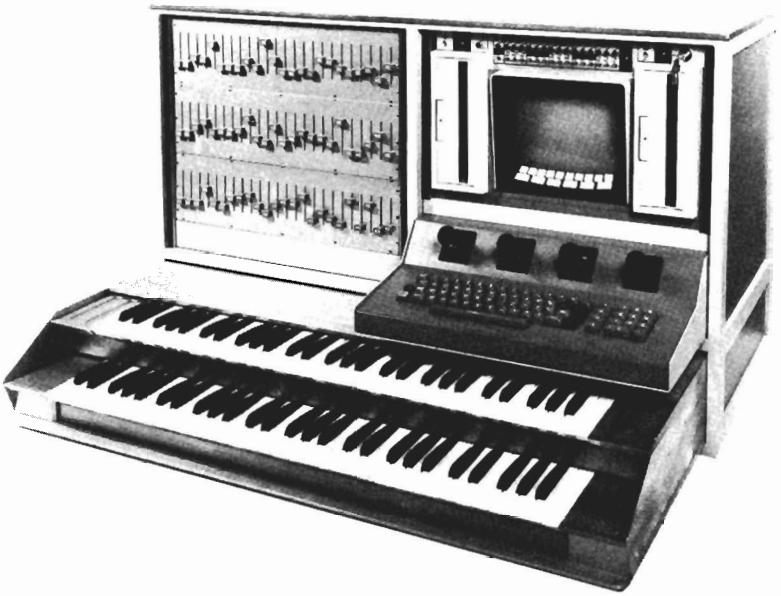


**Fig. 1-9. A digital synthesizer capable of linear fm.** *(Courtesy Bell Laboratories)*

and waveform animators. Much experimentation is now being done in this area. See Fig. 1–9. Many people believe that nonlinear techniques are the "wave" of the future because of the vast timbral changes available with a relatively small amount of circuitry.

### Subtractive Synthesis

The most popular technique of sound synthesis today is that of *subtractive synthesis*. In this method a waveform is generated that is usually rich in harmonics. This waveform is then acted on by filters and attenuators for the desired sound.

There are three basic functional building blocks in this synthesis approach: the waveform generator, or *oscillator*, the *filter*, and the *attenuator* (Fig. 1–10). All are usually *voltage controllable*. The frequency of the oscillator is controlled by a voltage from some controller, such as a keyboard. The oscillator waveform is then fed into a filter, which can also be controlled by some voltage source such as the keyboard. The output of the filter is then fed into an attenuator that is controlled by a voltage

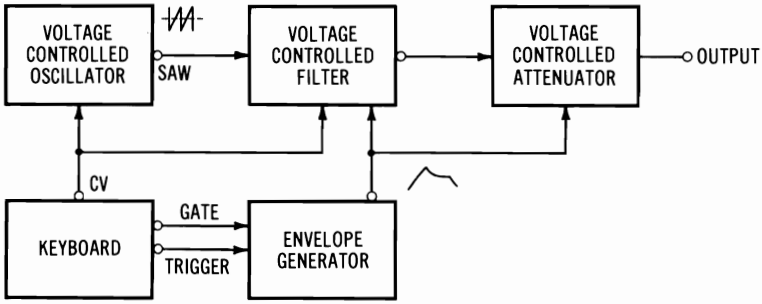



**Fig. 1-10. Subtractive synthesis—a minimal one-voice system.**

from an *envelope generator*. The envelope generator's output is initiated by timing signals from the keyboard. Its envelope is manually programmed with front-panel control knobs.

The subtractive technique is popular because of its instant programmability and playability. All parameters are variable and accessible on the front panel of the unit. Modules are programmed according to what you *hear*—not what you *heard*.

The main disadvantage of the subtractive technique is its sound. It sounds like a synthesizer and not a natural sound. This is because the frequency content of the sound is dictated by the oscillator waveform. Amplitude variations of frequency content can be performed by filters, but frequency relationships of the harmonic content are fixed by the content in the oscillator waveform. The recent introduction of nonlinear techniques, such as waveform animation, to the subtractive system has improved its capabilities immensely, and it is in subtractive technique where most advances in analog synthesis technology are being made.

The analog system design approach has been the most popular method of synthesis. Its functions, or *modules*, can be used to attempt small-scale additive or nonlinear synthesis, but they are most often arranged for subtractive synthesis.

Most functions in the system are voltage controllable. Rack-mounted systems package each function in its own separate module, each with its own set of inputs and outputs (Fig. 1-11). Arrangement of the modules in the rack is often left up to the synthesist. The modules are interconnected, or *patched*, using patch cords or matrix switches. Although this method

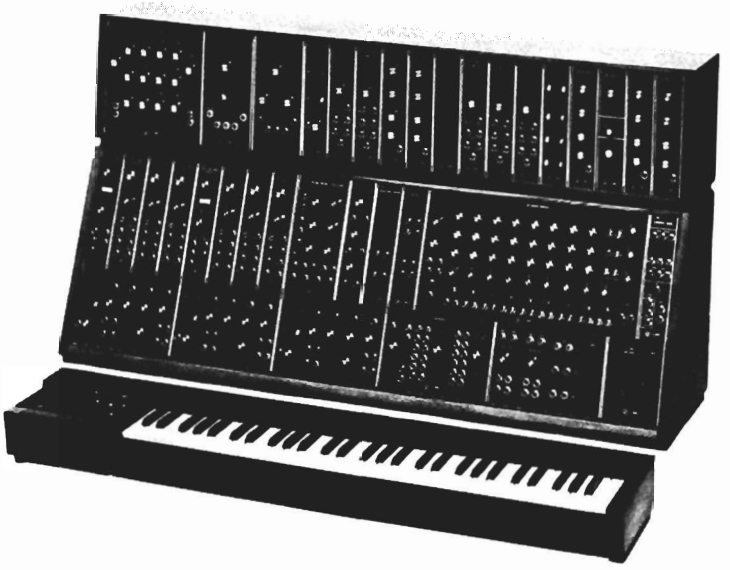


**Fig. 1-11. The Moog *System 55* synthesizer.** *(Courtesy Moog Music, Inc.)*

provides the most versatility and patching possibilities, it is not very practical in a live performance situation. Too much time (and memorization) is required to set up for a new sound. For the preceding reason, smaller synthesizers exist that contain the basic modular functions and leave out the lesser used "frills."

These smaller "performance" synthesizers consist of circuitry much like that of the larger, rack-mounted systems. Instead of having input and output jacks, however, the circuitry is wired together in the common "one-voice" configuration. These systems are *hard-wired* because there is very little patching that the user can perform. Some units do provide *some* auxiliary break points in the wiring to allow external connections.

These units usually have only one (*monophonic*) or two (*duophonic*) note capability. This feature may seem limited, but actually such a unit is a very powerful instrument although the "one note at a time" limitation forces the musician to develop his or her synthesis and keyboard technique to add character to his or her music.

A *polyphonic* synthesizer (Fig. 1–12) contains at least four separate "voices," which means that the synthesizer can generate at least four notes *simultaneously*. The operation is the same

**Fig. 1-12. The Sequential Circuits *Prophet 5,* a polyphonic synthesizer.**
*(Courtesy Sequential Circuits)*

as with monophonic synthesizers, except some sort of position rule or timing priority is required of the keyboard for keys down. This could be: first note played is assigned the first voice, second note the second voice, and so on. Usually all voices are programmed similarly to utilize the ensemble effect (see the following).

The newer synthesizers have patch memorization capabilities. Patch settings on the control knobs and switches are entered in digital memory and can be recalled at the push of a button. A typical system will memorize 20 patches or more. Once a patch is selected from memory, it can usually be modified and reentered in memory in altered form if desired. This type of synthesizer, although complex in design, is not very difficult to use and is really an exciting instrument to own and play.

Another type of snythesizer, often called the *string synthesizer*, uses tone generators and dividers for pitch generation. Some of the circuitry relates back to organ technology in design. A very high frequency waveform (often crystal controlled) is divided by a *top-octave generator* IC to output 12 high-frequency notes of an octave. These are then further divided down for the lower octaves (Fig. 1–13).

The active filter circuits that act on these notes are more elaborate than those found in organ circuits. Some units combine fixed filters with voltage controlled filters. A few units even have voltage controlled filters and voltage controlled attenuators for each key.

The sound is often enhanced by paralleling two tone-generating sections that are slightly out of tune. When two notes that are very near in frequency are mixed together, they audibly "beat" against each other. This is called the *ensemble* effect. It is a characteristic of natural instruments (ever tune a guitar?). This type of synthesizer is often designed to imitate string sections of an orchestra. Usually the sounds available are preset and may only be variable over a small tonal range.

## ANALOG SYNTHESIZER SYSTEM DESIGN

A nice feature of analog synthesizer construction is that you can start out small. You can put together one module at a time and build up the system slowly to coincide with your budget and leisure time. A minimum number of modules is required for interesting sound capabilities.

Before starting, however, you must set down some system guidelines and make sure the circuits you choose or design will conform to them.

### Linear and Exponential Voltage Relationships

If a graph is made of the relationships of note frequency to key position on a keyboard, the result will be an exponential curve (Fig. 1–14). The notes on the keyboard are arranged in twelve-note sequences called *octaves*. Seven of the notes (the lower, usually white, keys) are designated C, D, E, F, G, A, and B. The other five (usually black) keys are termed sharps (♯) or flats. The term *sharp* signifies that the note is higher in pitch. The term *flat* means that the note is lower in pitch. A♯ means that the note is higher in pitch than A but not as high as B. The "kicker" is that this note can also be called B flat. The two notes are the same. All notes are equally spaced in relation to the twelfth root of 2, or a frequency difference of about 6 percent. The frequency of A4 (above middle C) is 440 Hz. Note A♯ is 440 Hz multiplied by the twelfth root of 2 (1.059 . . . ), or 466 Hz. Note B is A♯ multiplied by the twelfth root of 2; and so on. Each higher octave is a factor of 2 higher in frequency. Thus the frequency of A5 is 880 Hz. This exponential relationship between note frequency and location must be duplicated by circuitry in the synthesizer.

One method would be to use an exponentially spaced resistor

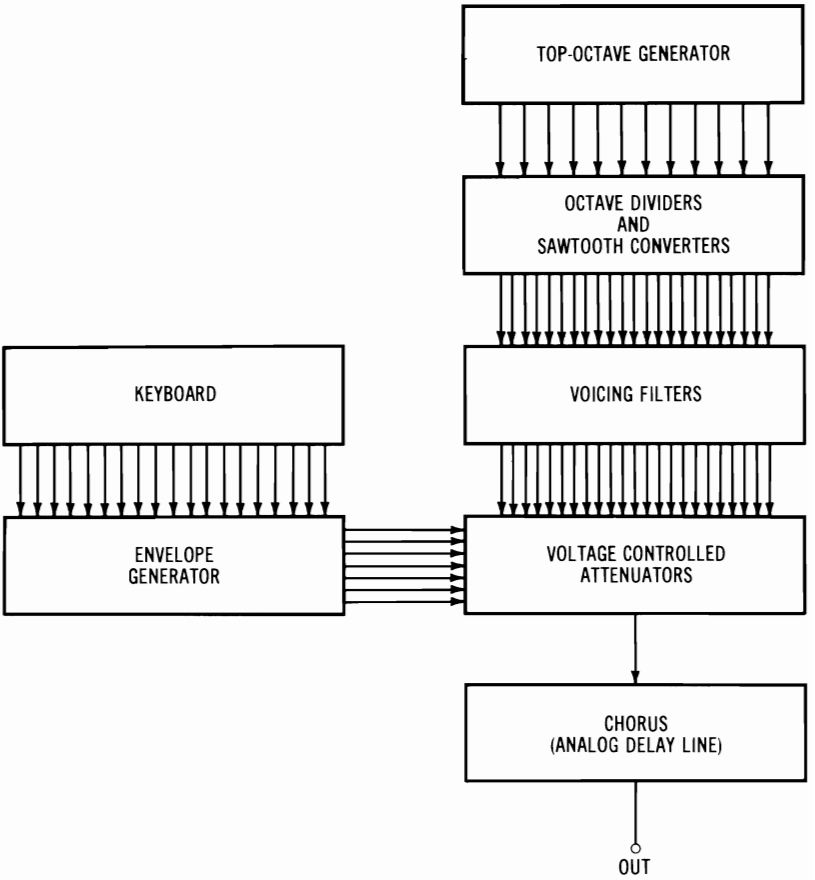



**Fig. 1-13. A typical string synthesizer block diagram.**

string in the keyboard. This requires precision resistors or, at least, sensitive tuning of variable resistor trimmers in the resistor divider string.

An alternative is to use an *exponential converter*. An exponential converter changes a linearly changing voltage into an exponentially rising one. Thus the keyboard resistor string can be made up of resistors of the same value for a linear output. This circuit then feeds into the exponential converter for the final output control voltage.

Using one exponential converter is not satisfactory. If two os-

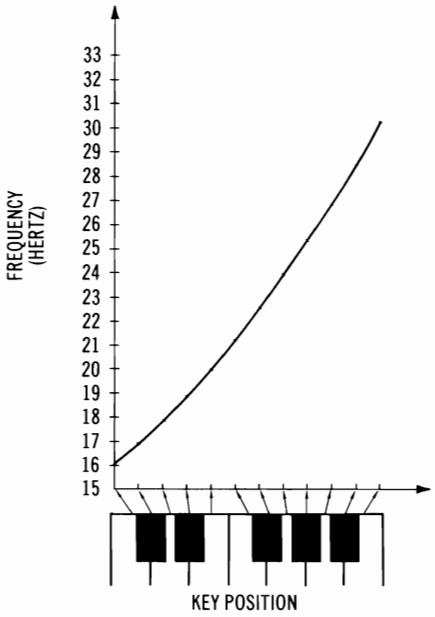



**Fig. 1-14. A graph of note frequency vs. key position.**

cillators are driven by the same exponential voltage and one oscillator frequency is manually offset from the others, the two oscillators will not track in frequency. The solution is to use an exponential converter (or exponential current source) at each module's input (Fig. 1–15). Most of the industry uses this method. If linear control is desired, it can be found as auxiliary inputs on many modules.

### Control Voltages

The standard control voltage ratio for the industry is *1 volt per octave*. One volt of control voltage causes a one-octave change in the module, whether it be the frequency of an oscillator or the cutoff frequency of a filter. This allows a ten-octave range for 10 volts, which is quite satisfactory.

### Timing Signals

In addition to providing one or more control voltages, the controller (keyboard) must output timing signals telling when keys are down and for how long. These pulses are then fed into various modules to initiate their functions (Fig. 1–16).

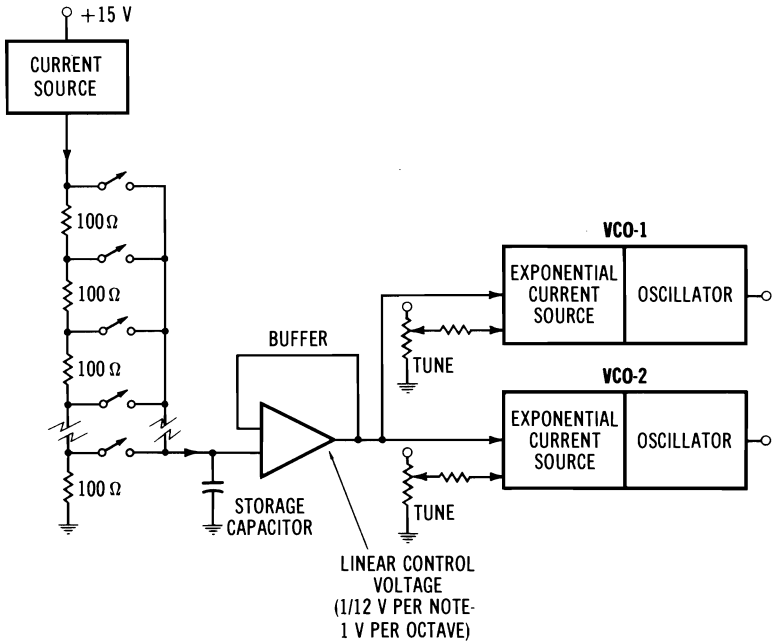



**Fig. 1-15. Synthesizer control voltage generation.**

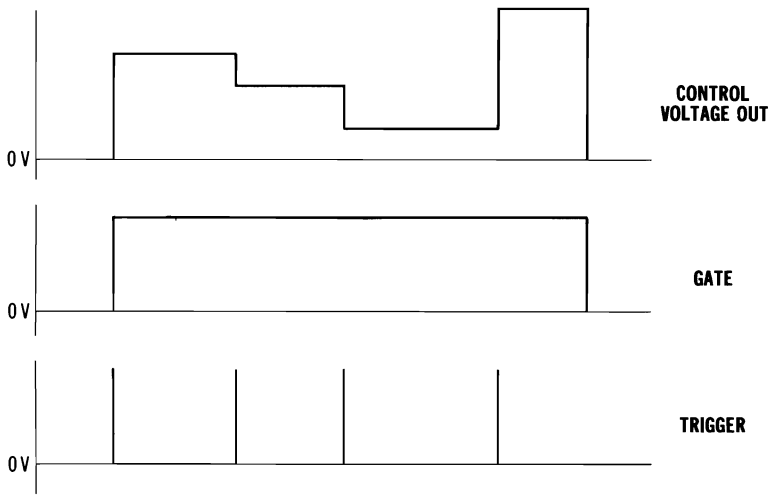



**Fig. 1-16. Keyboard timing signals.**

The most common timing signal is the *gate*. Its level is high whenever a key is down. It is used to initiate the envelope generator. When used with an ADSR-type envelope generator (see Figs. 1–17 and 1–18), it will start the attack portion of the envelope and, after the decay, will determine when the final release portion of the envelope will occur.

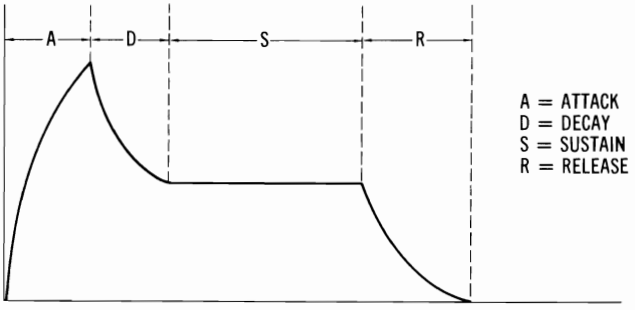



**Fig. 1-17. The ADSR envelope.**

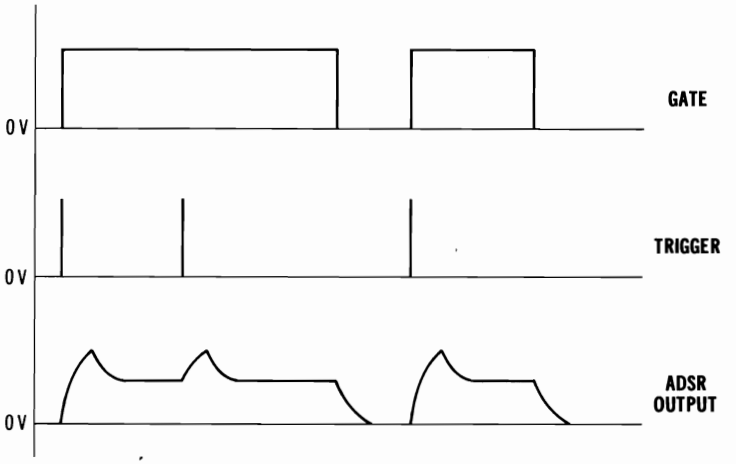



**Fig. 1-18. A timing diagram of an envelope generator.**

A second timing signal is the *trigger*. It occurs whenever a new key is pressed. It is a small, fixed-length pulse that is used to "retrigger" the envelope generator's output. When the envelope generator receives a trigger it will restart its envelope.

The trigger can also be used to trigger sample and holds or sequencers.

Most synthesizers use gate and trigger voltages that are at least as large in magnitude as the signal waveforms. Typically they are from 5 to 10 volts when high.

The module input accepting the timing signal(s) will usually consist of a Schmitt trigger or comparator. These circuits are level-sensitive circuits that change states when the input crosses a determined threshold. The typical threshold in many commercial synthesizers is 2 volts. Such an input structure allows slowly rising input voltages to act as trigger (or gate) sources.

### Input Structure

The most common input structure for control and signal voltages is the op-amp summing node. This is the "−" input with negative feedback. The circuit is basically an inverting summing stage.

The value of the 1 V/OCT control voltage input resistor is most often a 100-kΩ low-tolerance (0.1 percent) type for gain accuracy and stability. This aids in reliable tracking of modules within the synthesizer.

### Output Structure

The output structure usually consists of a low-impedance source followed by a 1-kΩ resistor. This 1-kΩ resistor protects the low-impedance source from shorts to ground which may accidentally occur when setting up a patch with patch cords. The resistor also allows passive mixing by directly wiring two (protected) modules' outputs together.

The only output that will not have a protection resistor will be the control voltage output. A 1-kΩ resistor in such a position would create a 1-percent error when fed into the 100-kΩ 1 V/OCT input of a module.

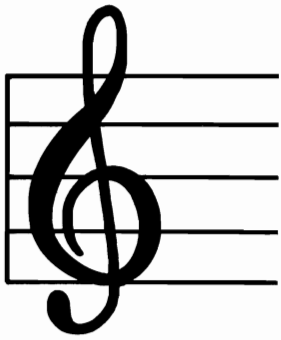
### Signal Levels

Most synthesizers output 10-volt peak-to-peak waveforms from the oscillators. However, the center of the waveform swing may be either 0 volts or 5 volts. This is because signal voltages are usually plus and minus 5 volts, and control voltages are usually 0 to 10 volts. Careful attention should be paid to these

signal levels because most module inputs are dc coupled. It will not do any harm to wire 0–10 V to an input meant for +/–5 V, but the result will probably not be as planned.

A level-translator module may be included in a system to allow oscillator waveforms to function as control voltages (0–10 V) as well as sound source signals (+/–5 V). Such a module would employ op amps to shift +/–5-V signals to 0–10-V signals.

# POWER SUPPLY CIRCUITS



# CHAPTER 2

A well-regulated power supply is necessary for stable synthesizer operation. Many critical exponential converter circuits derive their reference voltages directly from the power supply.

The majority of circuits found in this book and elsewhere use +15-, −15-, and +5-volt supplies. Circuits with other voltage requirements (such as +9, −9 or +12, or −12 volts) can usually be used with +15 and −15 volts with minor circuit changes.

A 1-ampere supply will satisfy the current requirements of most synthesizer systems. If your regulators are extremely hot to the touch, it is a sign that additional current capacity or heat-sink area is needed. A 1-ampere supply will typically power 20 or more modules. A module's current requirements can be roughly estimated by adding the circuit's IC quiescent currents (usually about 3 mA each) to the currents drawn by resistor dividers and op-amp loads. LEDs usually draw about 20 mA each, so it is advisable to limit their use unless you have the current to spare.

## THE REGULATED SUPPLY

A typical synthesizer power supply consists of an *unregulated dc source* followed by an *IC regulator circuit* (Fig. 2–1). The unregulated supply configuration will vary with the power transformer chosen. Typical transformer rectifier configurations are shown in Fig. 2–2.

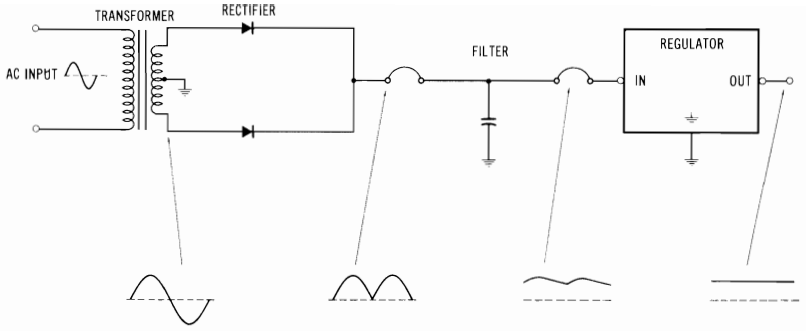



**Fig. 2-1. A basic power supply.**

## Regulator Input Characteristics

The input restrictions of the regulator determine the unregulated supply design requirements. IC regulators usually require an input dc voltage about 3 volts higher in magnitude than their specified output voltage. This voltage is called the *drop-out voltage* of the regulator. The output voltage will fall out of regulation if the input voltage falls below this level. The regulator also has a maximum input voltage rating, which is usually about 15 volts higher than the output voltage of the regulator. Operating with inputs higher than this level will result in a "blown" regulator. Thus, for a typical 15-volt regulator chip, the input voltage must be within the range of 18 to 30 volts.

Variations in the ac line voltage must be taken into consideration in the design of the unregulated supply. Variations in line voltage can cause the unregulated supply to fall outside the allowable regulator input voltage range.

## The Transformer

The voltage output of a transformer will vary, depending on its load. This is due to the voltage drop created by the resistance of the transformer secondary winding. With no load, very little current is drawn through the transformer and the output voltage is high. With a load, more current is drawn through the transformer and the output voltage is lower. Most manufacturers rate their transformers at full output current. These voltages are expressed as rms (root-mean-square) voltages, which are 70.7 percent of the peak voltages. Typical no-load to full-load voltage

output variation is about 20 percent. With a light load, the output may be high enough to cause the regulator input voltage to be above its maximum allowable value.

Secondary current ratings should be at least 1.2 times the load current for the full-wave center-tap configuration and 1.8 times the load current for the full-wave bridge configuration. For twin 15-volt supplies a 36-volt ct (center tapped) transformer is frequently used. For 5-volt supplies a 12.6-volt ct filament transformer is popular.

### The Rectifier

The diodes in the rectifier circuit must be able to handle the average current drawn by the load as well as any surge currents due to turn-on transients or output shorts. In full-wave rectifier circuits each diode passes an average of one-half of the output load current. However, the rms ripple current into the filter is at least twice the output current. The magnitude of the rms current increases as the ripple voltage decreases. By increasing the size of the filter capacitor in the power supply design, the ripple voltage will decrease. Also, when the supply is first turned on, the filter capacitor acts as a short circuit. During this time the current is limited only by the secondary resistance of the transformer. Therefore the rectifier diodes must be able to handle this current surge.

A good practice is to use diodes of at least twice the average dc current drawn by the load. For the majority of circuits 1-ampere diodes are sufficient.

The peak reverse voltage (prv or piv) rating of the rectifier diodes should be at least twice the peak output voltage of the transformer.

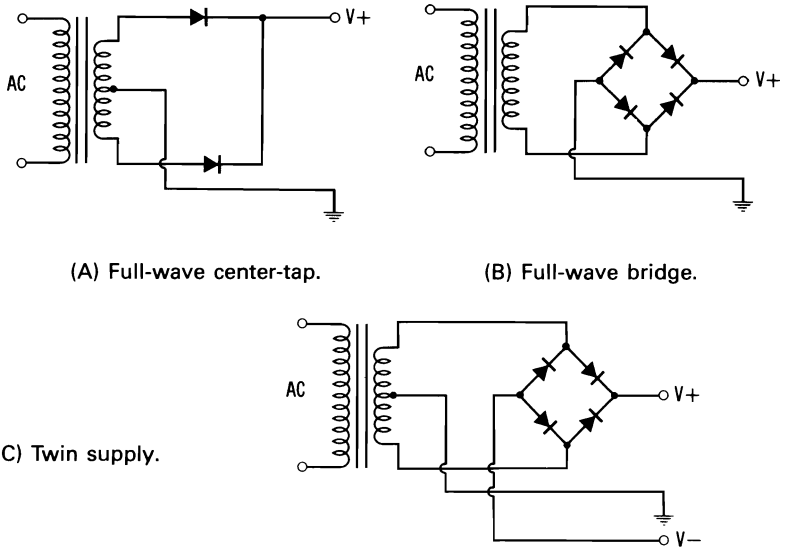
For a full-wave, center-tapped transformer configuration (Fig. 2–3) the peak output voltage is

$$V_{pk} = \frac{1.414V_{rms}}{2} - V_{rect}$$

where

$V_{rms}$ is the secondary rms voltage at full load,

$V_{rect}$ is the voltage drop across the diode at full load, approximately 1.25 V, not 0.6 V.




(A) Full-wave center-tap.

(B) Full-wave bridge.

(C) Twin supply.

**Fig. 2-2. Typical transformer/rectifier configurations.**

For a transformer with an untapped secondary in a full-wave bridge configuration (Fig. 2–2B) the peak output voltage is

$$V_{pk} = 1.414V_{rms} - V_{rect}$$

where

$V_{rms}$ is the secondary rms voltage,

$V_{rect}$ is the voltage across the diodes at full load, approximately 2.5 V in this case.

A 100-volt-prv diode is satisfactory for most applications since $V_{pk}$ is usually less than 30 volts (maximum input of the regulator).

Heat sinking of the diodes is accomplished by their axial leads. Therefore leads should be kept short and should be soldered to large traces on the circuit board.

## The Filter Capacitor

The choice of filter capacitor will depend on the rectifier voltage output and the amount of ripple voltage the regulator will tolerate. The ripple voltage is decreased and the average dc voltage is increased as the capacitance of the capacitor is in-

creased. Most regulators have high ripple-rejection ratios (large ripple in, small ripple out), allowing the ripple to be fairly large. Such a design has a high peak voltage to make up for the current output of the filter capacitor in between charging intervals. The regulator has to work hard (it will generate heat) to regulate this voltage down to the regulated output level. A circuit designed with less ripple (larger filter capacitor) has the peak voltage (which is set by the transformer secondary voltage) closer to the drop-out voltage of the regulator. The regulator will have to work less since its input is closer to the desired output voltage.

A formula to determine the value of the filter capacitor (Fig. 2–3) is

$$C = \frac{I_L \times 10^6}{120V_{rip}}$$

where

$C$ is the capacitance in microfarads,

$I_L$ is the maximum load current in amperes,

1/120 second is the time interval between charging cycles at a frequency of 120 Hz.

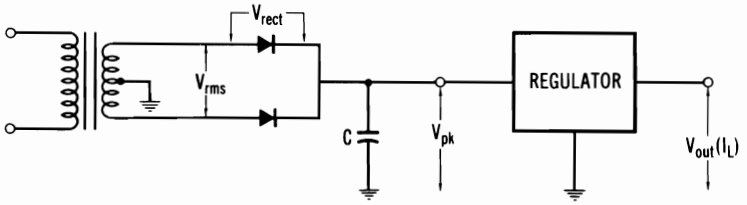
$V_{rip}$ is the ripple voltage in volts, which can be a maximum of $V_{pk} - (V_{out} + 3)$, where $V_{out}+3$ is the drop-out voltage.

## IC REGULATORS

The majority of common IC regulators are of the series pass design, as shown in Fig. 2–4. A voltage reference ($V_{ref}$) is compared with the regulator output voltage ($V_{out}$). The comparator notes any difference in voltage and adjusts the bias on the base of the series pass transistor for more or less conduction. Usually, a low-value resistor is placed in series with the transistor output. As the load draws more current from the supply, the voltage across this resistor increases. As the output current approaches the specified maximum output of the regulator, this voltage turns off the series pass transistor. Often included in the IC design is a temperature-sensing circuit that shuts down the regulator if it gets too hot.

### Heat Sinks

IC regulators require heat sinking when the load current is 20 percent or more of the maximum rated output. If the heat sink is




**MINIMUM REQUIRED SECONDARY CURRENT (RMS):**
FULL-WAVE CENTER-TAP CONFIGURATION = $1.2 \times I_L$
FULL-WAVE BRIDGE CONFIGURATION = $1.8 \times I_L$

**Fig. 2-3. A full-wave center-tapped power supply.**

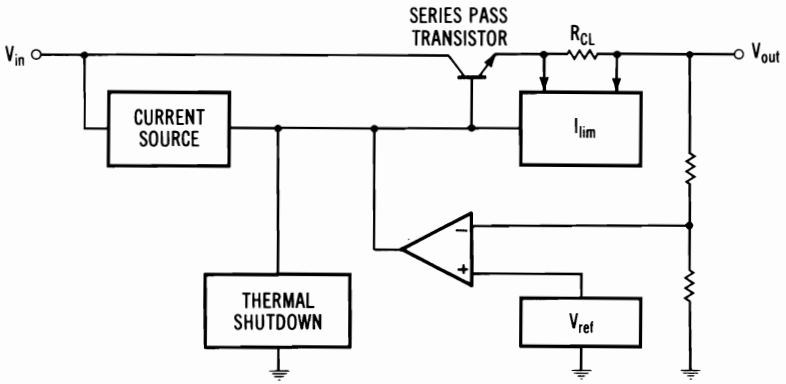



**Fig. 2-4. A series IC regulator circuit.**

too small, the regulator will get very hot and shut itself off (if it has that capability). For small-current applications the power supply chassis can serve as the heat sink. For load currents larger than 500 milliamperes, however, separate heat sinks should be provided. These can often be obtained from surplus sources or can be made from aluminum extrusions.

## Regulator Types

There are two types of IC voltage regulators: *fixed-voltage* and *adjustable*. The fixed-voltage regulator has all of the circuitry shown in Fig. 2–4 on the chip. It is available in several

output voltages. Fixed regulators are low in cost, easy to use, and can be used with external components for higher-current, adjustable, or tracking twin supply circuits. Low-power versions are available for local, on-card regulation.

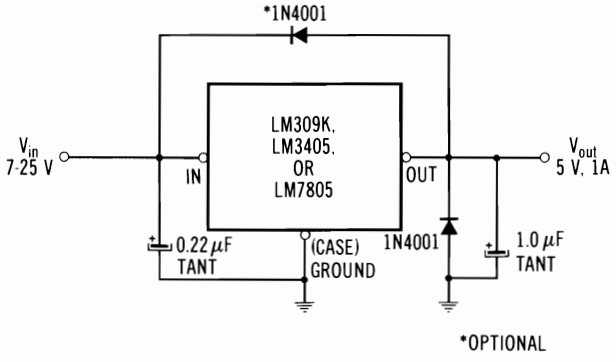
Adjustable voltage regulators are often very similar to fixed regulators in design, with the exception that the voltage reference is adjustable and/or external. In addition, the current limiting function can sometimes be controlled externally. A disadvantage of fixed regulators is that output voltages will often vary ±2 percent or more with different production lots. Adjustable regulators can be easily adjusted to the desired voltage. For example, the LM317 adjustable regulator can be set for any voltage between 1.2 and 37 volts with specifications equal to, or better than, those of fixed regulators.

### Stability and Protection Circuitry

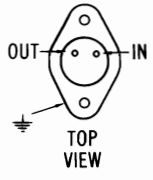
IC regulators usually require a few external components for reliable operation. A capacitor is required from the input terminal to ground to help eliminate possible stability (oscillation) problems. The suggested type of capacitor varies. Often it is suggested as a tantalum electrolytic of about 2 $\mu$F. Tantalum capacitors are becoming expensive and hard to find, however. They are chosen for their relatively low internal resistance at high frequencies. A possible substitution for the tantalum capacitor is a 25-$\mu$F aluminum electrolytic in parallel with a 0.1-$\mu$F or larger disk ceramic. In either case, place the capacitor(s) as close to the regulator leads as possible.

Some regulators also require a capacitor from the output terminal to ground. This capacitor is often a 1-$\mu$F tantalum or a 25-$\mu$F aluminum electrolytic. A 0.01-$\mu$F ceramic should be added in parallel to minimize high-frequency noise.

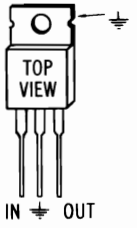
If there is any chance of the unregulated supply being shorted, a *protection diode* should be placed from the input to the output on positive regulators (Fig. 2–5). If a short occurs, the current stored in the output capacitor(s) will flow through the diode rather than through the regulator, thereby destroying the diode. This diode is provided internally in most negative regulators. Diodes are also needed across the outputs of regulators in a bipolar supply to ensure proper start-up during turn-on with a common load between outputs.




(A) Circuit.




(B) K package.




(C) T package.

**Fig. 2-5. A 5-volt, 1-ampere, fixed-voltage regulator.**

## Fixed-Voltage Regulators

Fig. 2–5 shows a common 5-volt, 1-ampere fixed-voltage regulator circuit. Its performance is similar with the LM309K, LM340–5, or the LM7805. If the filter capacitor is more than 4 inches away from the regulator use a tantalum-type capacitor (0.2 $\mu$F or larger). The output capacitor should be at least 1.0 $\mu$F and tantalum. If tantalum capacitors are hard to find, you may try a 25-$\mu$F aluminum electrolytic in parallel with a 0.1-$\mu$F ceramic type as suggested earlier. A protection diode may be necessary to prevent latch-up with negative loads.

Fig. 2–6 shows a twin 15-volt, 1-ampere, fixed-voltage regulator power supply. Its performance is similar with either regulator listed. Take care when mounting the negative-voltage regulators to heat sinks: the case is not ground but the input.

Fig. 2–7 shows a tracking supply using fixed-voltage regulators. The trimpot in the negative supply is adjusted for a

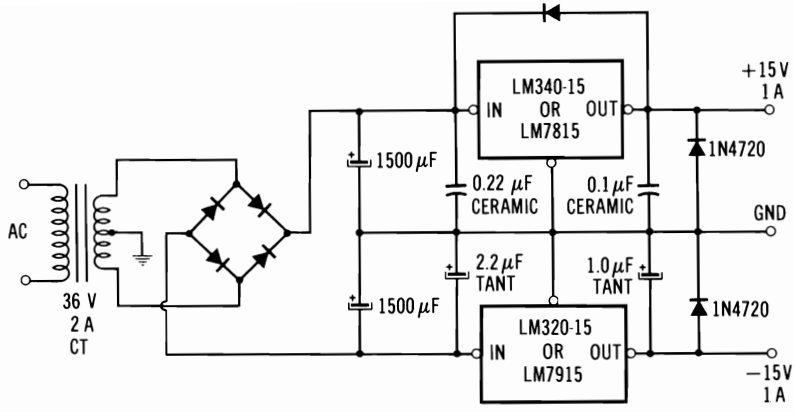



**Fig. 2-6. A +/−15-volt 1-ampere fixed-voltage regulator supply with short-circuit protection diodes.**

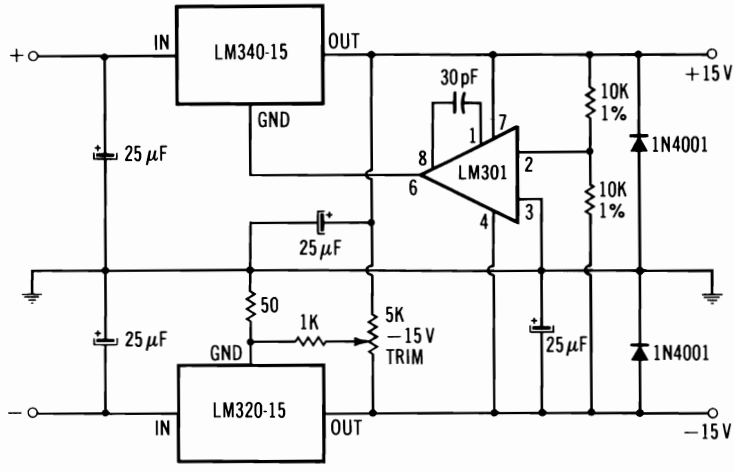



**Fig. 2-7. A +/−15-volt, 1-ampere, tracking regulator supply.** *(Courtesy National Semiconductor Corp.)*

−15-volt output. The positive supply will track the negative supply.

## Adjustable-Voltage Regulators

A very popular adjustable-voltage regulator IC with superior specifications and a low price is the 723. A functional pin dia-

gram of the 723 is shown in Fig. 2–8. The current limit and output voltage (2–37 volts) are set externally. A voltage reference is provided within the chip and is brought out on pin 6. The available output current of the IC is a maximum of 150 milliamperes. External pass transistors can be added for higher output currents.

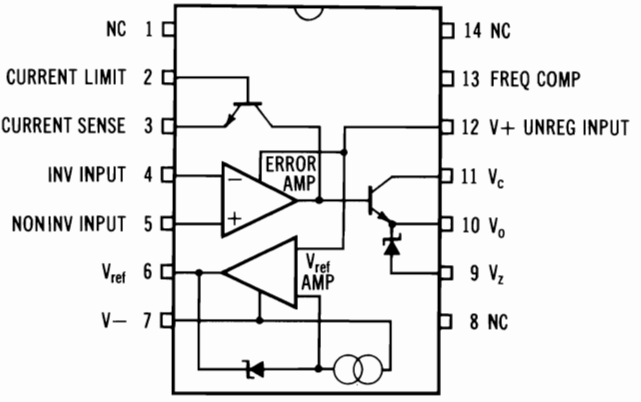



**Fig. 2-8. A functional diagram for the 723 voltage regulator.**

Fig. 2–9 shows a twin supply using the 723. When a twin supply is made from two positive regulators, ground connections of the two circuits must be kept separate except for a single common ground connection at the output. A center-tapped transformer may not be used. In the circuit of Fig. 2–9 the transformer has two separate secondary windings. Another method is to use two separate transformers. Capacitors C3 and C8 reduce ripple on the $V_{ref}$ output (pin 6 of the 723s). Resistors R1 and R6 improve temperature stability. The components in the voltage divider network should have low temperature coefficients for low output voltage drift with ambient temperature variations.

The positive supply of Fig. 2–10 is similar to the one in Fig. 2–9. The negative supply is unique, however. As the positive supply rises in amplitude due to load variations, the voltage at the negative input to the op amp (previously 7.5 V) will also rise. As this voltage rises, the op amp senses a difference in potential between the "+" and "–" inputs. It then tries to correct this at its output, pin 6. This causes the op amp to draw

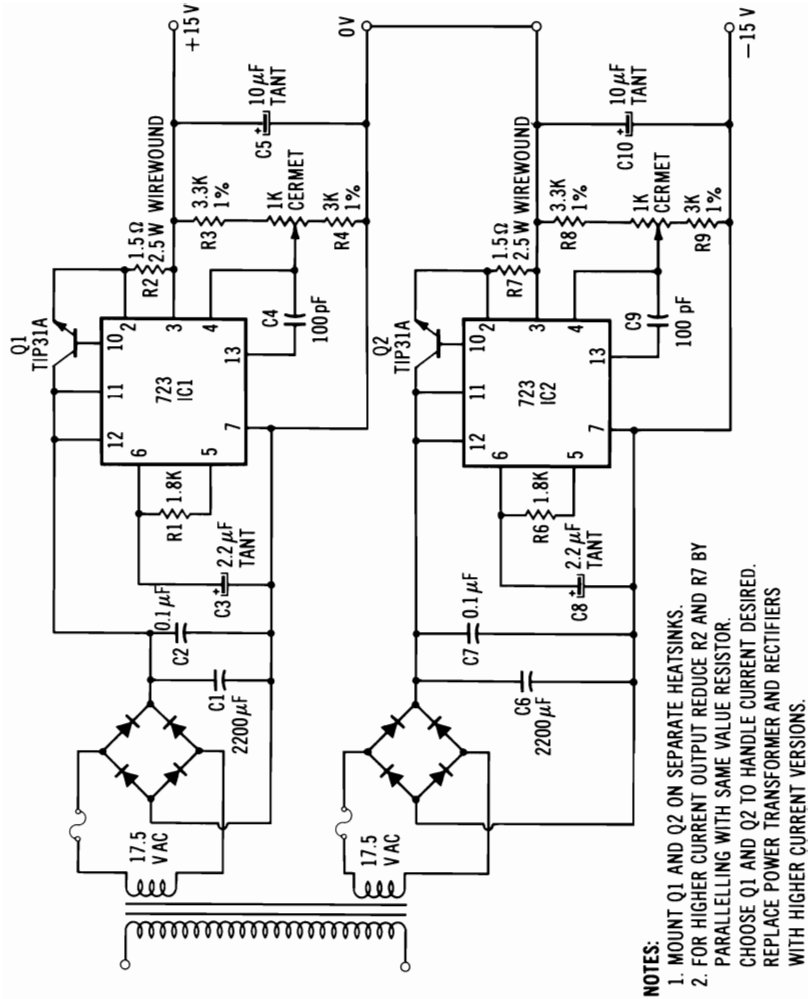



**Fig. 2-9. A +/−15-volt (nontracking voltage regulator) supply.**
*(Courtesy* ETI Magazine *and Digisound, Ltd.)*

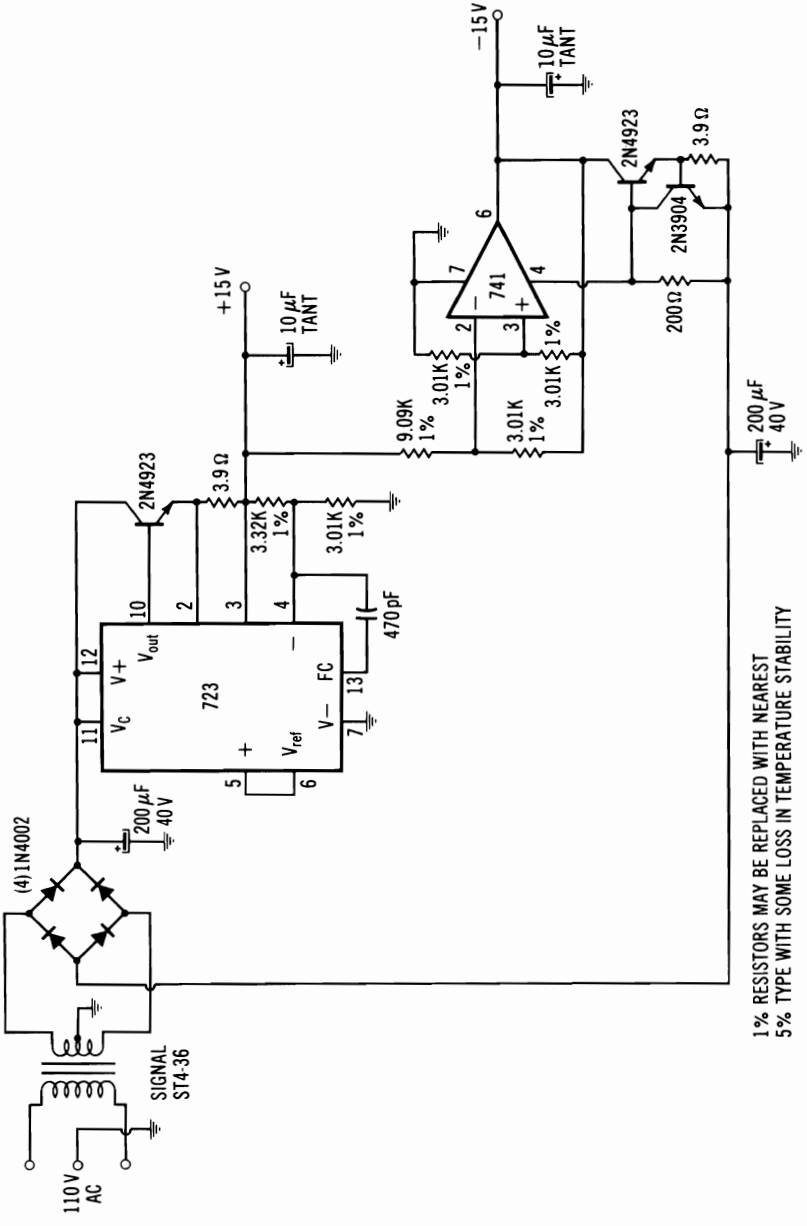


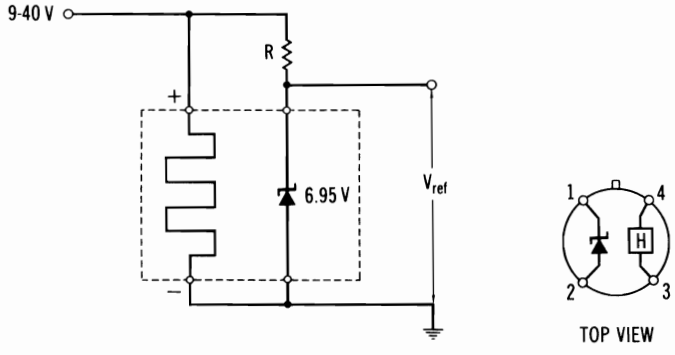

**Fig. 2-10. A +/−15-volt tracking power supply.** *(Courtesy Solid State Micro Technology for Music, Inc.)*

more current and the voltage drop across the 200-ohm resistor increases. This voltage turns on the 2N4923 transistor, making the output more negative. The 3.9-ohm resistor acts as a current-limit sensor. As the output current increases, the voltage drop across this resistor increases, causing the 2N3904 to turn on and cut off the 2N4923 when the output current gets too high.

## SUGGESTIONS

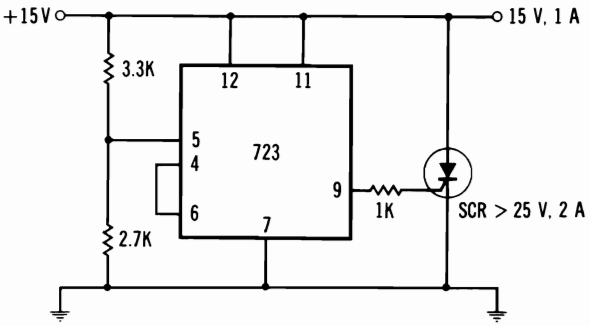
When building your synthesizer, you will need both a test bench power supply for prototyping and a synthesizer power supply for completed modules. You could start out having your bench supply perform both functions and later, as you have completed several modules, construct a dedicated synthesizer supply.

The circuit of Fig. 2–6 would make a good supply for either purpose. It is inexpensive to build and is identical with many commercial synthesizer supplies. The 723 circuits provide better regulation performance and, with modifications, higher current output. They can also have very good thermal stability due to their ability to accept an external voltage reference. A good voltage reference for this application is the LM399H. It is a precision 6.95-volt reference that has excellent thermal stability (Fig. 2–11).

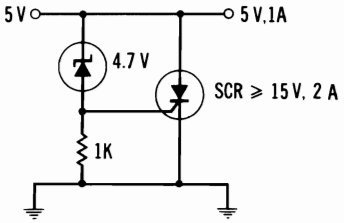



(A) Circuit. (B) Top view.

**Fig. 2-11. The LM399 precision voltage reference.**




(A) With SCR and resistors.

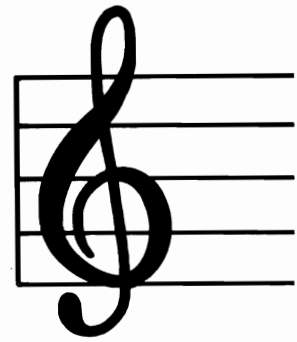



(B) With SCR, resistors, and zener diode.

**Fig. 2-12. Power supply protection circuits.** *(Submitted to* Electronotes by Dave Rossum)

Protection circuits, such as those shown in Fig. 2–12, are suggested on all power supply. outputs. These circuits detect any intersupply shorts and short the output of the supply to protect against damage to the regulators and to ICs in the synthesizer circuitry. The SCRs in these protection circuits must be rated to handle the full current output of the supply. You may wish to install LED power indicators (with appropriate current-limiting resistors) on the supply outputs to indicate their proper function.

# CONTROL VOLTAGE GENERATORS, PROCESSORS, AND CONTROLLERS



# CHAPTER 3

Analog synthesizers are dependent on control voltages for proper operation. These control voltages can vary from a voltage taken from a front-panel *coarse tuning* control to several 1 V/octave control voltages and timing signals from a polyphonic keyboard.

The interface between a musician and his or her synthesizer is called a *controller.* It converts some form of physical motion, stimulus, or activity into control voltage(s) and/or timing signals. Traditional controllers include the keyboard, the foot pedal, and the ribbon controller. Some of the newer types include proximity sensors, biofeedback circuits, and ambient sound analyzers.

*Control voltage generators* output a control voltage that is either random, periodic, or predetermined. The *envelope generator,* the *sequencer, noise sources,* and *low-frequency oscillators* (lfo's) fall into this category.

The control voltage outputs from envelope generators and sequencers are largely preprogrammed by the musician and occur in response to an external trigger. Noise sources and lfo's generate a control voltage independent of external stimuli.

*Control voltage processors* derive control voltages and/or timing signals from an input waveform. *Sample and holds, slew limiters, trigger and gate extractors,* and *envelope followers* fall under this category.

A sample and hold accepts an input signal and stores a control voltage in response to a trigger. A slew limiter outputs a signal

that is a slew limited (increased rise and fall times) version of its input. A trigger and gate extractor generates timing signals if its input surpasses a certain dc level. An envelope follower accepts an input signal and outputs a dc level according to the input signal's average amplitude with time.

## CONTROLLERS

### Keyboards

The most common controller for a synthesizer is the keyboard. Its circuitry is referred to as the *keyboard interface.* Most inexpensive synthesizers have a one-voice, or *monophonic,* keyboard. The output signals of this keyboard consist of a 1 V/octave *control voltage,* a *gate* signal, and a *trigger* signal (review Fig. 1–16).

The control voltage is a dc level that corresponds to the position of a key pressed on the keyboard. The voltages for each key occur in linear steps, 1/12 volt apart, for 1 volt per octave. Some keyboard circuits allow the ratio of volts per octave to be altered with a "range" control. This provides the capability to play microtonal scales.

The keyboard control voltage output remains at the dc level of the last key played even after the key is released. Often it is desired to have notes last longer than a key is held down. The constant key voltage causes the vco(s) to continue oscillating at the frequency of the last note played. If the envelope generator has been set up for a long decay time, it will cause the note to last even longer after the key is released. Most monophonic keyboards will output a dc control voltage for the lowest note played if more than one key is held down. This is called *low-note priority.*

Most synthesizers have a feature called *portamento.* Increasing portamento lengthens the amount of time the control voltage takes to change from one key voltage to another. With no portamento the change is instantaneous and the abrupt change in oscillator frequency is obvious. With a moderate amount of portamento the glide from note to note becomes apparent (see Fig. 3–1).

When one or more keys are depressed a gate signal is generated. This is a timing signal that is interfaced to an envelope generator. When a key is pressed the gate output goes high, ini-

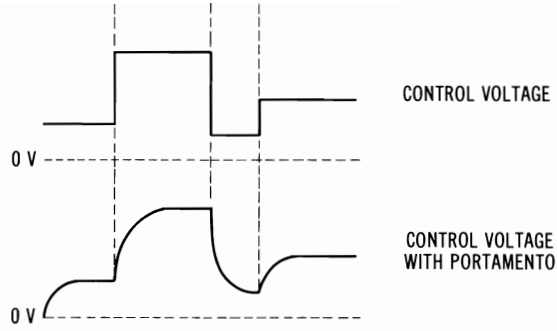



**Fig. 3-1. Portamento's effect on keyboard control voltage.**

tiating the envelope generator's output. If an ADSR envelope generator is used, the envelope will sustain at the SUSTAIN level set as long as the gate signal is high. Once the gate signal goes low (key(s) released) the final "release" portion of the envelope will begin (see Figs. 1–16, 1–17, and 1–18).

At the initial actuation of a key some keyboards also output a trigger pulse. This is a small-duration pulse ($\approx$ 5 ms) that is also interfaced with the envelope generator to signal that a key has been depressed or key position has changed. The trigger pulse is vital in the case (monophonic keyboard) where one key is pressed and then a lower key is pressed. Without a trigger pulse signifying a key position change (lower key) the envelope initiated by the gate could be completed by the time the key position changed, thus you wouldn't hear the second note. The trigger is required to reinitiate the envelope generator and can only occur if the gate is high (see Fig. 1–18).

*Duophonic* keyboards have two-voice outputs (two control voltages and timing signals).

*Polyphonic* keyboards have several voices. The circuitry here is complex because of the necessity to prevent "voice jumping" that would occur if a lower note is released while higher keys are still depressed. Most of the circuitry is digital in polyphonic interfaces. Some units contain a microprocessor to allow keyboard splitting, inverting, and note sequence memorization in addition to the standard interface functions.

In addition to generating control voltage(s) and timing pulses some synthesizers have *velocity-sensitive* and/or *pressure-sensitive* keyboards. Velocity-sensitive keyboards output a per-

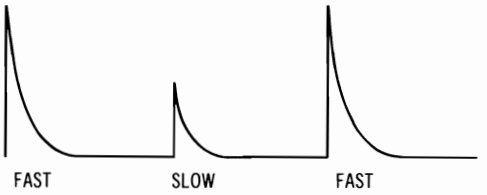
cussive voltage that increases in level with the speed that a key is pressed. This voltage is often fed into the voltage-controlled amplifier to momentarily increase the output volume as the keys are pressed. Pressure-sensitive keyboards output a voltage that increases as keys are pressed harder. This voltage can then be used to control output volume or modulation of some sort. Fig. 3–2 shows typical outputs of such keyboards.

## A Monophonic Keyboard Approach

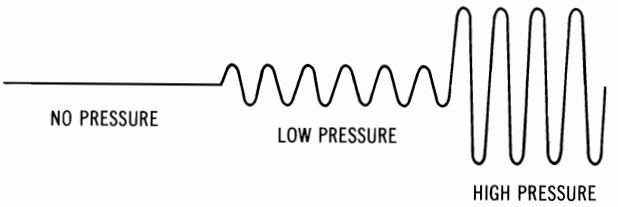
Fig. 3–3 shows a monophonic keyboard interface for a one-bus keyboard. It is a modified version of a circuit designed by Bernie Hutchins.[1]

A *constant-current source* (A1, Q1) drives the keyboard resistor string. A constant current ensures a constant voltage drop across each divider resistor even if more than one key is held down. Resistor R2 trims the key voltage interval to 1 volt per octave. The "tune" control (R5) raises or lowers the overall keyboard tuning. The resistors in the keyboard divider network should all be the same value in the range of 50–200 ohms (1 percent). The optimum design value is 100 ohms.

The keyboard voltage is buffered by A5. Resistors R6 and R7 and diode D4 cause the output of A5 to be −0.7 V if no keys are




(A) Velocity sensitive.




(B) Pressure sensitive.

**Fig. 3-2. Keyboard control voltages.**

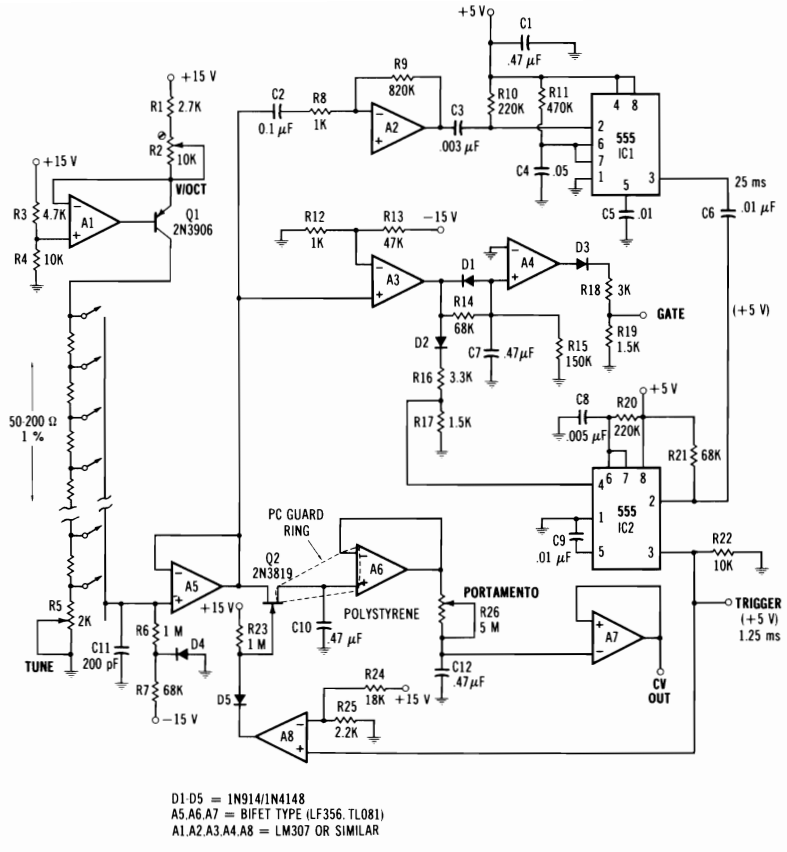



**Fig. 3-3. A monophonic keyboard interface for a one-bus keyboard.**

pressed. Capacitor C11 filters out noise on the bus line. The A2 circuitry acts as a differentiator. Any change in control voltage pulsed through C2 and R8 is amplified by A2. These pulses are input to IC1, which is a one-shot monostable that triggers on a negative input pulse. Once this monostable is triggered, IC1 pin 3 remains high for about 25 ms.

Op amp A3 acts as a comparator in this circuit. It goes high any time the voltage on the positive input rises above the voltage on the negative input pin (which is set by R12 and R15). The voltage on the negative input is set at about 0.35 V, half way between ground and the −0.7-V output of A5 when no keys

are pressed. Possible A5 key control voltage outputs range from 0 volts (R5 shorted) to several volts, depending on the keys pressed and their octaves. The −15- to +15-V level output of A3 is converted to a 0- to 5-V level by D2, R16, and R17. A 5-V level into IC2 pin 4 enables IC2 and allows the pulse from IC1 to cause a 1.5-ms trigger pulse out on pin 3.

Diode D1 and resistors R14 and R15, along with capacitor C7, delay the rising level of A3, causing comparator A4 to output a delayed −15-V to +15-V level. This level is converted to a 0- to 5-V level by D3, R18, and R19. This output is the gate.

The trigger output (pin 3) of IC2 is input to comparator A8. This −15- to +15-V level turns on the sample-and-hold FET, Q2. This allows the keyboard control voltage to be stored by C10 and buffered by A6. The output of A6 is fed to the portamento circuit of R26 and C12. This is buffered by A7 for the final control voltage output.

If the gate voltage were not delayed by A4, the synthesizer's envelope generator would be activated before the new keyboard control voltage was set up on the sample and hold. This would cause the old pitch to be heard for a short interval if a fast attack setting was used on the envelope generator. The signal timing of this circuit is shown in Fig. 3–4.

The basic advantage of this circuit is that it allows the use of inexpensive (possibly surplus) one-bus keyboards. The control voltage is more susceptible to drift than other designs using more than one keyboard bus due to the *droop rate* of the sample and hold. Droop rate is the rate at which the storage capacitor looses its charge. The key voltage is sampled only once and for a very short time for each key depression. After the trigger samples the sample and hold, C10 begins to discharge at a rate dependent on the input bias current of A6, the type of capacitor used for C10, and whether the printed circuit layout around C11 and A6 is clean of contaminants. A guard ring is shown on the schematic. This is an actual printed circuit trace on the board that encircles the traces leading from the top of storage capacitor C10. The guard ring is connected to the negative input of A6. Since the level on this guard ring is the same as that on C10 (but at a lower impedance) there is less leakage from C10. Other circuits, using more than one keyboard bus, gate the sample and hold on with a second bus. Thus droop rate does not become a factor until a key is released.

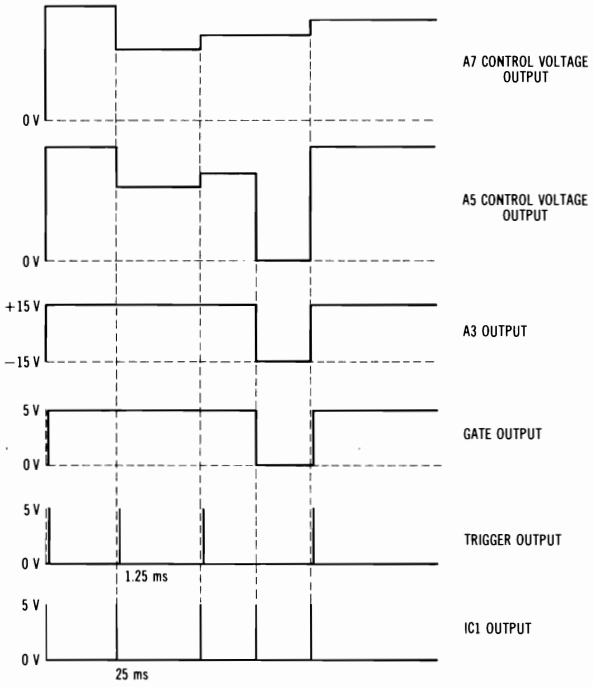



**Fig. 3-4. Voltages for Fig. 3-3.**

## A Duophonic Interface

The circuit of Fig. 3–5 is a duophonic, 3-bus, keyboard interface that appeared in *CFR Technotes*.[2]

Op amp A3 and transistor Q7 form a constant-current source much like the one in the circuit of Fig. 3–3. Op amp A5 buffers the level of the voltage on the bus. The wire from the voltage bus to A5 is shielded to eliminate any 60-Hz line noise from entering the circuit. The first voice gate signal originates from a separate keyboard bus. It turns on sample and hold FET Q8 whenever a key is down. Op amp A4 buffers the voltage stored on the control voltage/portamento capacitor.

The portamento circuit in this design performs differently than the circuit in Fig. 3–3. In Fig. 3–3 the control voltage changes in abrupt steps at the output of A6. The output of A7 will always eventually reach the same level of A6 at a rate determined by the setting of R26. In Fig. 3–5, however, if the first voice key is released, FET Q8 turns off and the voltage remains

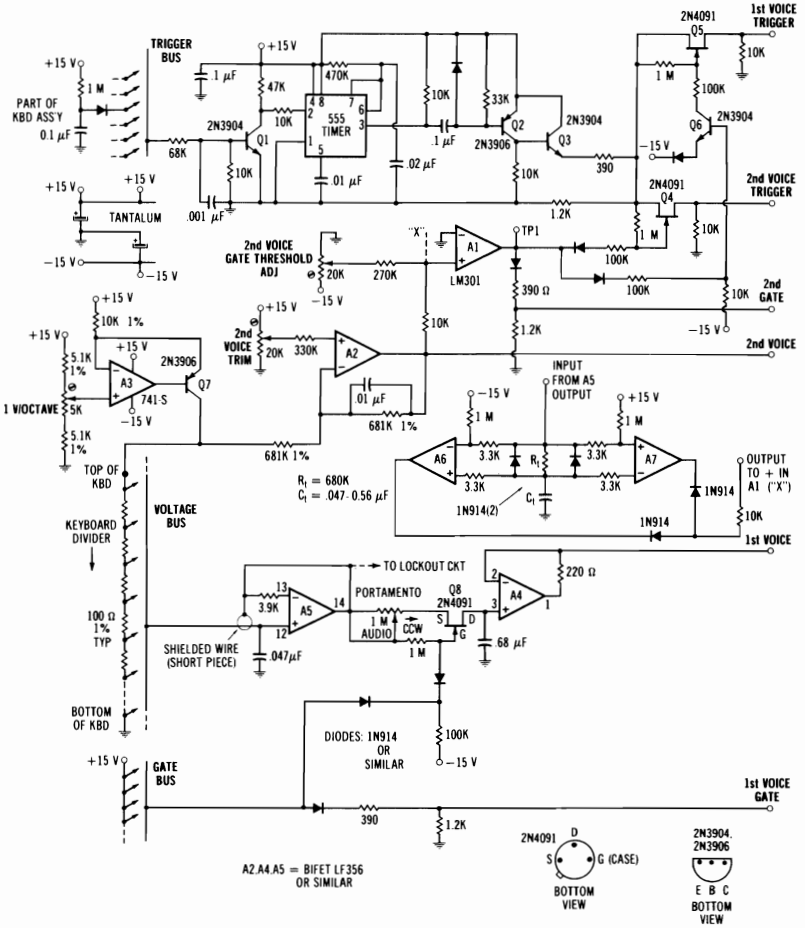



**Fig. 3-5. A three-bus, duophonic, keyboard interface.**

constant on the storage capacitor. The portamento glide will stop.

The second voice trimpot is adjusted until the output of A2 is 0 when no keys are pressed. Whenever two keys are held down the voltage at the top of the keyboard will change to keep a constant current on the resistor divider network. The voltage difference will be output to A2. When this voltage is summed with the first voice control voltage at the input of a vco, the vco will follow the second voice or upper key pressed.

A third keyboard bus pulses Q1 whenever keys are pressed. Transistor Q1 triggers the 555 one-shot to output a 5-ms pulse. The negative-going edge of this pulse is inverted by Q2 and buffered by Q3. The pulse is then fed into FET switches Q4 and Q5. When there is no second voice, comparator A1 outputs −15 volts, turning the first voice FET, Q5, on and turning off the second voice FET, Q4. When there is a second voice, A1 will output +15 volts, turning off first voice FET Q5 and turning FET Q4 on. Thus the trigger pulse is gated to the correct voice trigger output.

The second voice trigger lockout circuit (A6, A7) prevents the second voice from retriggering if the second voice is held down and a series of notes is played on the first voice. It consists of two comparators that sense a difference between the voltage stored on $C_t$ and the control voltage output from A5. As long as the first voice is changing these voltages will be different due to the charging time of $R_t$ and $C_t$. This locks out the second voice trigger.

The gate bus of this circuit could possibly be eliminated by using a comparator referenced close to ground to monitor the trigger bus. Any time a key is pressed the comparator would go high, generating a gate signal and enabling the sample and hold.

For proper operation of this circuit, the key control voltage bus must be the first to make and the last to break contact. This ensures that the control voltage is ready to be loaded into the sample and hold before the gate signal appears. Also, clean contacts are a necessity with all keyboard interface circuits. Contacts can be cleaned with rubbing alcohol and cotton swabs.

### Control Voltage Ranging and Scaling

The circuit of Fig. 3–6 shows a control voltage ranging and scaling unit.[3] This circuit allows easy adjustment to scales other than 1 V/OCT. Also, manual adjustment of overall tuning is provided with coarse and fine pots. The keyboard interface is first adjusted for 1 V per octave. This is best done with the V/OCT switch in 1 V/OCT and the coarse and fine controls in midposition. Measure the output of A4 with a dvm for 1 V per octave or calibrate by ear alternately playing two notes an octave apart while listening to a calibrated vco.

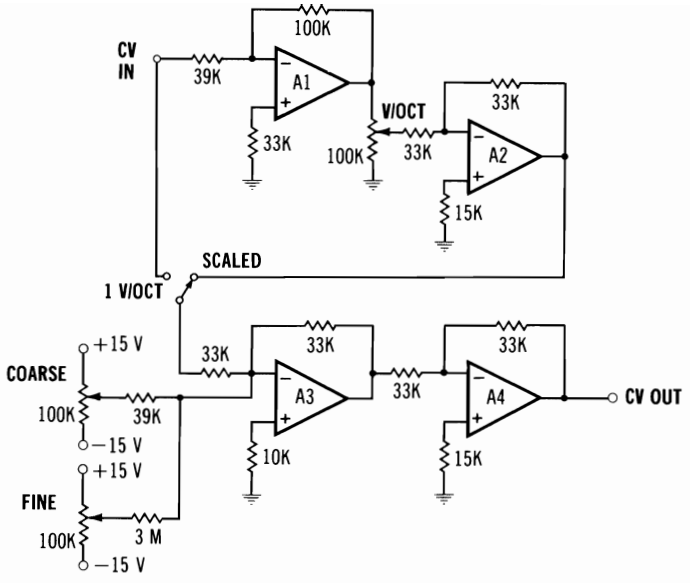



**Fig. 3-6. A control voltage ranging and scaling unit.** *(Courtesy Electronotes)*

## Joystick

A joystick interface circuit is shown in Fig. 3–7. A joystick allows control over two parameters with one control. The second voice lockout circuit (A6, A7) of Fig. 3–5 could possibly be used in conjunction with this circuit to provide a gate signal whenever the joystick is moved.

## A Pressure-Sensitive Controller

The black conductive foam used to protect static-sensitive ICs from damage during handling and/or shipping can prove to be a useful material for controllers. The resistance of the material varies with its density. If a piece of the foam is placed between two metal plates the resistance between the two plates will decrease as the foam is compressed. This forms the basis of a pressure-sensitive controller.

Fig. 3–8 shows a circuit for such a pressure-sensitive controller. Resistor R1 sets the overall gain of the circuit. If the output voltage range is too large or too small, change the value of R1.

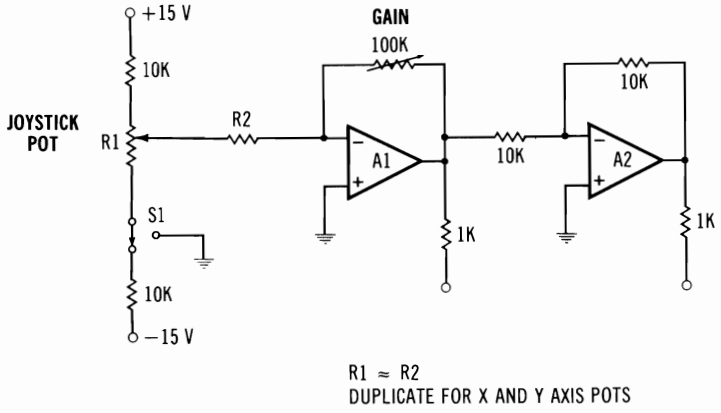



**Fig. 3-7. A joystick interface circuit.**

### A Ribbon Controller

A ribbon controller can be made using conductive foam. This is shown in Fig. 3–9. A strip of foam is laid out on a nonconductive surface. Metal conductors are glued to the ends of the foam strip. A piece of aluminized Mylar film is fixed above the conductive foam. Pressing down on the Mylar film will cause it to contact the foam and pick off the voltage at that point. This voltage is then applied to interface circuitry for a final control voltage output. The circuitry of Fig. 3–3 can be used by substituting the ribbon controller for the keyboard.

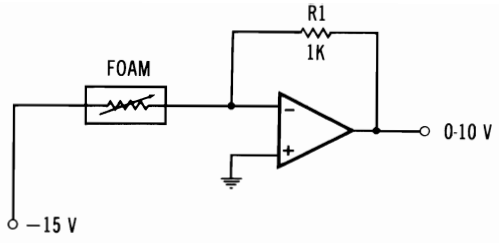
## CONTROL VOLTAGE GENERATORS

### Envelope Generators

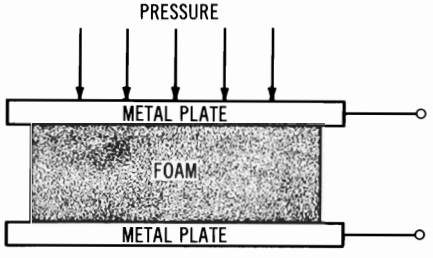
An envelope generator generates a control voltage or envelope that is usually nonperiodic. The envelope, initiated by a timing signal, begins at 0, rises to some positive level, and then falls back to 0.

There are several types of envelope generators, including the attack-release (AR), the attack-decay (AD), and the popular attack-decay-sustain-release (ADSR).

Fig. 3–10 shows a basic attack-release (AR) circuit. The storage capacitor (C1) is charged at a rate determined by its capacitance and the setting of the ATTACK control (R1). Capacitor C1 discharges through D2 and DELAY control R2. The




(A) Circuit.




(B) Construction.

**Fig. 3-8. A pressure-sensitive controller.**

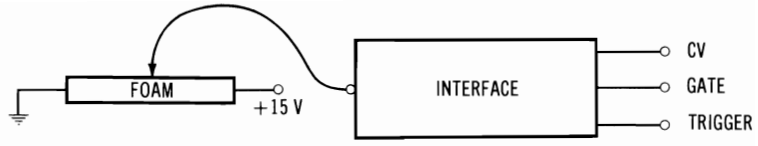
charge and discharge rates are exponential. The time $T$ it takes for $C$ to charge or discharge to 63 percent of the input voltage is determined by the time constant formula:

$$T = RC$$

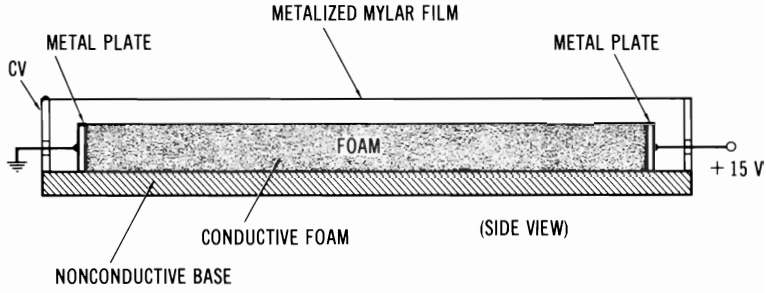
where
$R$ is in ohms,
$C$ is in farads.

After this first time period, it will take another $T$ to reach 63 percent of the remaining input voltage level. Diodes D1 and D2 allow separate attack and decay settings.

Fig. 3–11 shows an attack-decay (AD) envelope generator circuit. A gate signal is sent to this circuit, which generates an envelope that rises to a maximum dc level and immediately begins to decay. Once triggered by the gate signal, it will generate its preset envelope even if the gate signal goes low before the envelope has been completed. The RC network on the gate

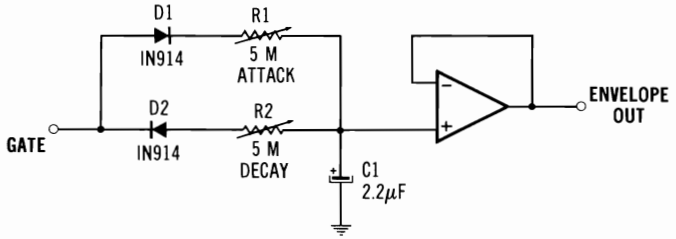



(A) Circuit.

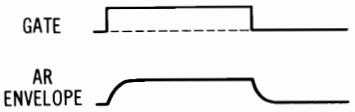



(B) Construction.

**Fig. 3-9. A ribbon controller.**




(A) Circuit.




(B) Waveforms.

**Fig. 3-10. An attack-release (AR) envelope generator.**

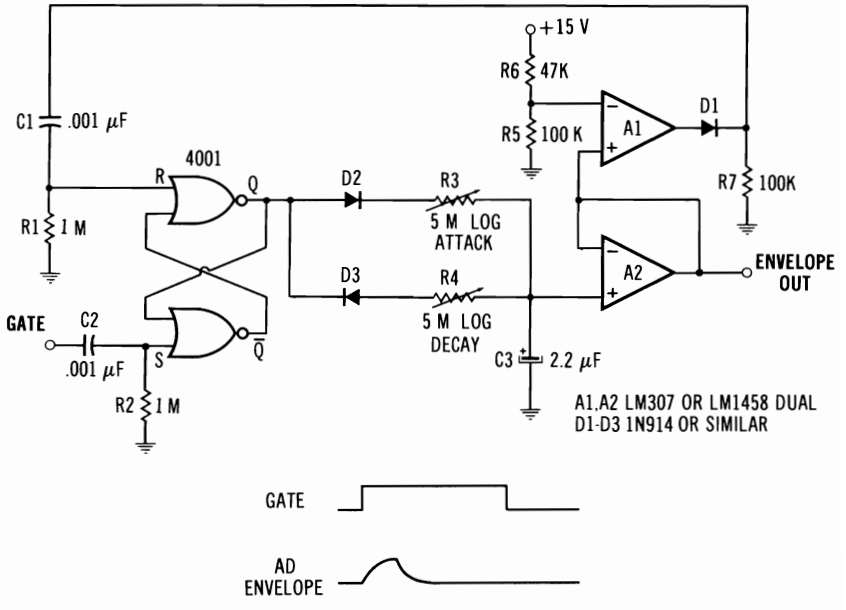



**Fig. 3-11. An attack-decay (AD) envelope generator.**

input causes a pulse to be generated, setting the Q output of the RS flip-flop (4001) high. This 15-volt signal (the CMOS uses a +15-V power supply) passes through D2 and R3 and charges C3. Op amp A2 buffers the voltage on C3. As this voltage rises above 10 volts, the output of comparator A1 will go high (15 volts). Diode D1 protects the output of the comparator (A1) and passes this voltage to C1 and R1. This causes a pulse to be generated which resets the RS flip-flop, so the Q output goes to a logic 0. Capacitor C3 then discharges through R4 and D3.

Fig. 3–12 shows an ADSR envelope generator. Initially, with no gate signal (ground potential), the output of comparator A3 is a logic 0. This causes the Q output of the RS flip-flop to stay at a logic 0. When the gate signal goes to a logic 1 comparator A3 goes to ground potential. The RS flip-flop state does not change but output NOR gate No. 1 goes to a logic 1, turning on analog switch 1 and initiating the attack portion of the envelope. The output of comparator A2 then goes to +15 V as the voltage on the storage capacitor C1 rises above 10 volts. This sets Q output of the flip-flop to a logic 1. NOR gate No. 1 and S1 turn off, and

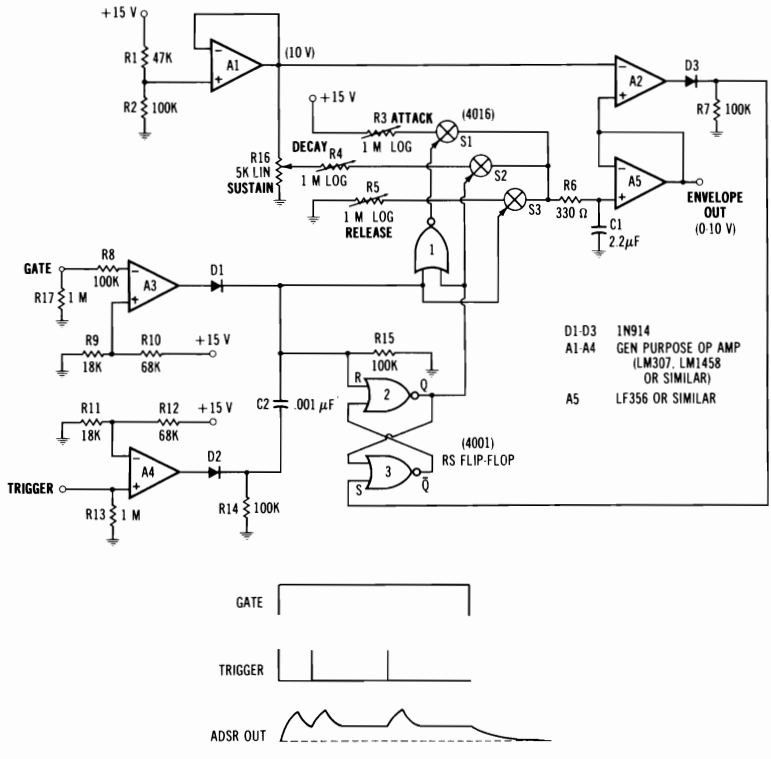



**Fig. 3-12. An ADSR envelope generator using analog switches.**

S2 turns on. The voltage on C1 is then discharged through the decay control (R4) to a dc level set by the sustain control (R16). When the gate signal goes to a logic 0, the Q output of the flip-flop goes to a logic 0. Switch S2 is then turned off, and S3 is turned on, initiating the release portion of the envelope. Retriggering the envelope is made possible by allowing a pulse from comparator A4 to reset the flip-flop, causing the output of NOR gate No. 1 to be a logic 1. The attack and initial decay portions of the envelope will then be repeated.

Fig. 3–13 shows a gate delay circuit which is almost identical with a circuit design by Bernie Hutchins in *Electronotes*.[4] As the gate goes to a logic 1, the output of A1 goes to a logic 0. This causes a negative pulse to appear at the input of NOR gate No. 1. This pulse is inverted by NOR gate No. 1, and again by NOR gate No. 2. This pulse triggers the 555 monostable, causing a pulse to be

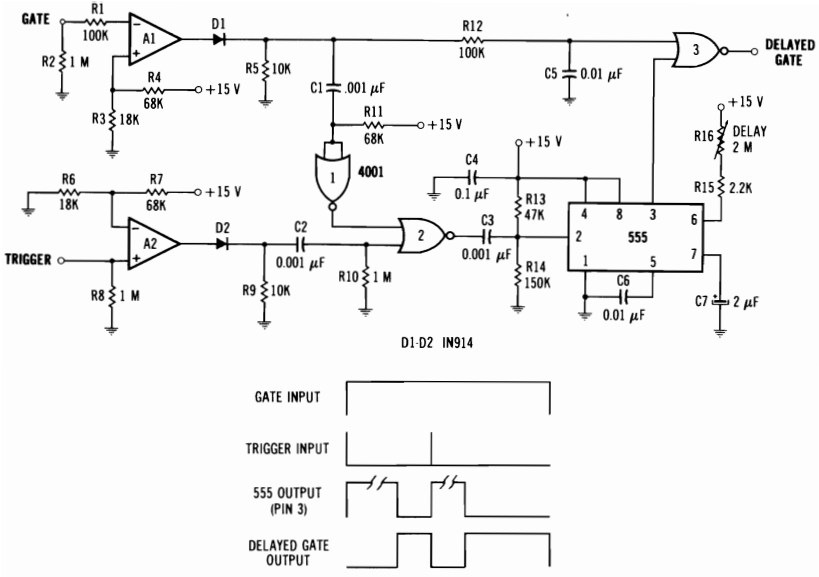



**Fig. 3-13. A gate delay circuit.**

generated with a duration set by delay control R16. Resistor R12 and capacitor C5 delay the gate signal to NOR gate No. 3 to compensate for the normal delay between the rising edge of the gate and trigger signals input to the circuit. When a gate signal is initiated, NOR gate No. 3 will be at a logic 0 for the duration of the pulse output of the 555 timer. After this period it will switch to a logic 1, lasting for the duration of the gate signal. A trigger input will retrigger the delay if a gate signal is present.

Recently, custom ICs for electronic music applications have been introduced that make the design and implementation of circuits much easier. One of the first chips that was available is the Solid State Micro Technology for Music (SSM) SSM2050 voltage controlled transient (envelope) generator chip. It is a full ADSR envelope generator with a 0- to 10-V output level. It has a 10,000 to 1 (1 ms to more than 10 seconds) time range, with an internal exponential converter providing an input control voltage sensitivity of 60 mV per decade. The sustain range is linearly controlled from 0 to 100 percent.

Fig. 3–14 shows an ADSR circuit using the SSM2050 designed by R.C. Blakey of Digisound Ltd.[5]

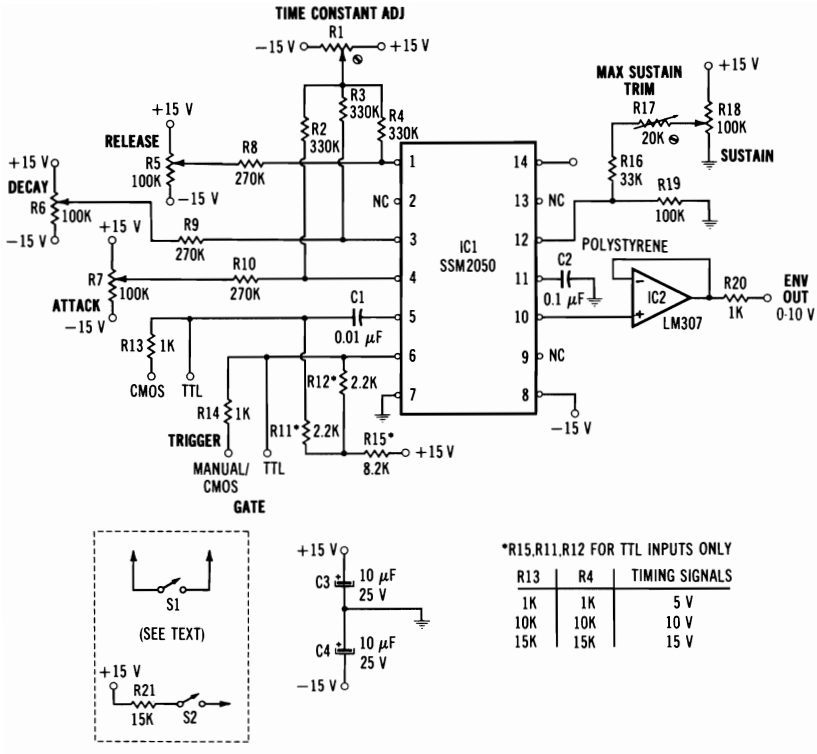



**Fig. 3-14. An ADSR envelope generator using the SSM2050.**
*(Courtesy* ETI Magazine *and Digisound, Ltd.)*

If CMOS level timing signals are used, S1 is connected across the CMOS trigger and gate inputs to allow both ADSR (S1 closed) and AD (S1 open) output contours. Manual gating is accomplished by adding a momentary-contact switch (S2) and resistor R21 to the manual gate input. If TTL timing signals are to be used, resistors R11, R12, and R15 must be added to the circuitry. Also, S1 must be moved to the TTL gate and a push-to-break switch should be connected between the TTL gate input and ground for a manual gate circuit.

The maximum sustain voltage out of the SSM2050 can possibly rise above the attack voltage of the envelope. This may cause the IC to malfunction, so R17 must be adjusted so that the maximum attack and sustain levels are equal (in the ADSR mode).

Quite a large variation in device characteristics can occur between different SSM2050 chips due to variations in input impedance. This impedance can be measured with a high-impedance ohmmeter between pins 1 and 7. Typical input impedance is 3.1 kΩ. Matching will be required if several 2050s are to be used in a system. Also, time constants can vary ±50 percent between devices. Devices can be matched, however, by setting all controls to their minimum settings and adjusting R1 for an attack time of 2 ms.

Fig. 3–15 shows an ADSR circuit using the SSM2055, an improved version of the SSM2050. The SSM2050 has a timing range of 50,000 to 1, minimum. An exponential converter is also contained in the chip, as was the case with the SSM2050. All input control voltages are positive (referenced to ground) with an input sensitivity of 60 mV per decade. The gate and trigger input circuits can accept a variety of input levels where the logic threshold is at about 2 V. Unit-to-unit time constant variations are greatly reduced—eliminating the necessity of selecting ICs for polyphonic systems. The SSM2055 was designed with polyphonic systems in mind, because the control input pins can be ganged with other units.

In the circuit of Fig. 3–15, provision is made for external control. As the control voltage increases, the attack or decay time will increase. Controls R1, R3, R5, and R7 are limited by resistors, so that a maximum of 10 volts can be output. This voltage or the external control voltage is then buffered and fed into a divider network voltage network, such as R13 and R14. This network sets the control range. If other control voltage ranges are to be used (such as 0–5 V), the network resistor values will have to be altered. Low-value resistors are recommended for R14, R16, and R18 when the divider is driving more than one SSM2055. The sustain level trimpot (R9) adjusts the maximum sustain dc level to be equal to the maximum attack level. The time constant trimpot (R20) is adjusted to match time constants between separate units. This is done by matching the maximum attack times between units. If the envelope generator is not to be used with other units, the trimpot can be eliminated and pin 2 should be grounded. A control voltage (perhaps the 1 V/OCT from the keyboard) into resistor R23 can be added to control all time constants of the IC simultaneously. Output buffer A1 is included as a safeguard. The SSM2055 has the capability to

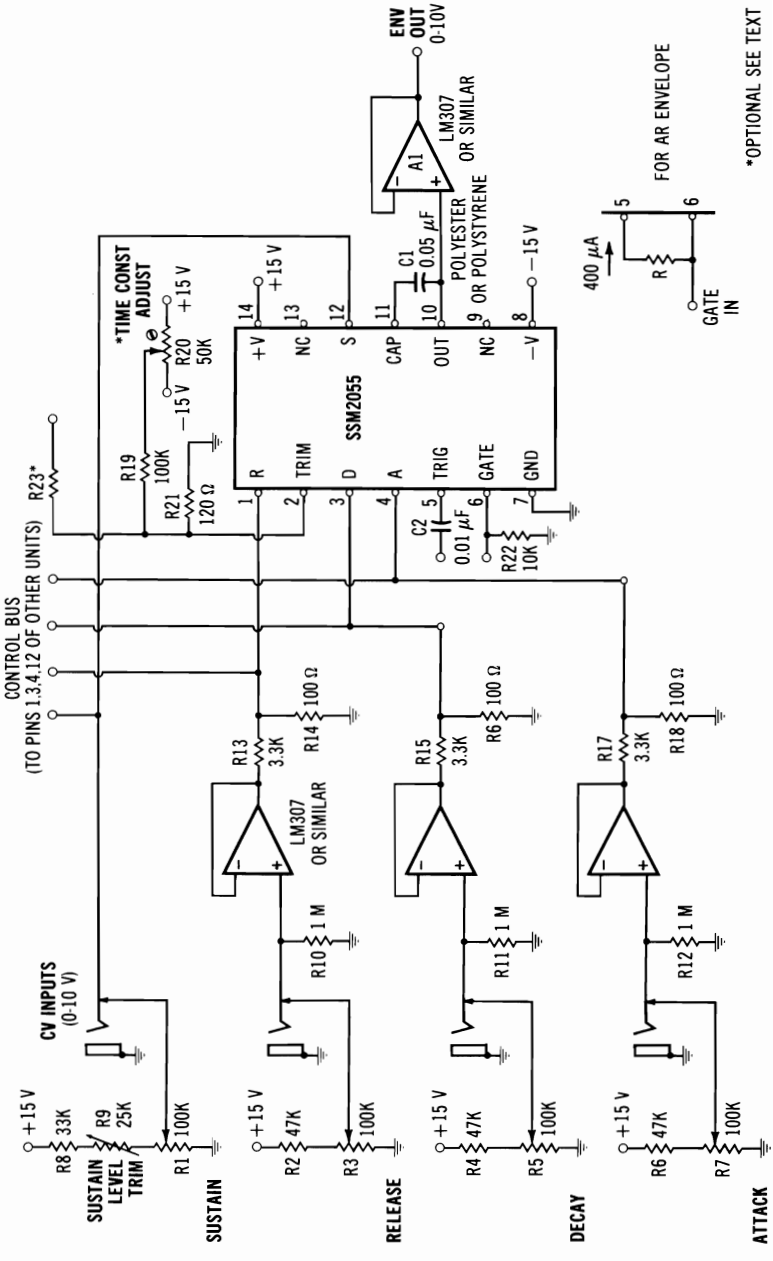



**Fig. 3-15. An ADSR envelope generator using the SSM2055.**

drive a 2.5-kΩ load with less than 5000 pF. Capacitor C1 is the storage capacitor for the circuit and should be a polyester or polystyrene capacitor for good stability.

Fig. 3–16 is a similar circuit for an ADSR envelope generator designed by R.C. Blakey of Digisound.[6] The circuit uses a Curtis Electromusic Specialties CEM3310 IC. The control voltages into the "attack," "release," and "decay" inputs of the CEM3310 can range from 0 to −5 volts. Increasingly negative voltages will result in longer attack, decay, and release times. The sustain input requires a positive voltage of 0 to +5 volts. This voltage will be the sustain voltage of the output envelope. Control input pins of similar tracking units in a polyphonic system may be ganged. One input attenuator can then control several ICs. The time constants of CEM3310s can vary ± 15 percent and can be matched using a trimmer (PR1).

In the circuit of Fig. 3–16, IC2A, IC2B, IC2C, and IC3A invert and attenuate the incoming control voltages. A voltage connected to EXT CONTROL A, D, and R will change the attack, decay, and release time constants simultaneously. Circuit IC3A inverts and attenuates the sustain voltage and IC3B inverts it again to the proper voltage range (0–5 V) required by the CEM3310. Pin 3 of the CEM3310 outputs the attack peak threshold voltage internal to the IC. Circuit IC3C limits the maximum sustain voltage on pin 9 at this level, preventing a voltage jump that would occur if the sustain voltage was higher than the internal peak attack voltage.

The internal output buffer of the CEM3310 has a relatively high output impedance. Performance is improved if it is buffered, as with IC5A. Circuit IC5B converts the CEM3310s normal 0–5 V output to 10 V. The attack output pin (pin 16) shifts from 0 V to a negative voltage (−0.4 to −1.2 V) when the circuit is in the attack phase. This turns on comparator IC6A and LED 1. Comparator IC6B turns on LED 2 whenever a gate signal is present. The gate signal is fed directly into pin 4. The trigger input signal in this circuit is derived from the gate signal by C8 and R4. This also triggers monostable IC1A and IC1B with an output pulse duration set by RV1. The output of the monostable is converted to a second trigger pulse by R5, C10, and IC1C. In the delay mode (S1 open) only this pulse goes to the CEM3310. The circuit then functions as an AD generator. With S1 in the retrigger position, this second trigger pulse is mixed with the

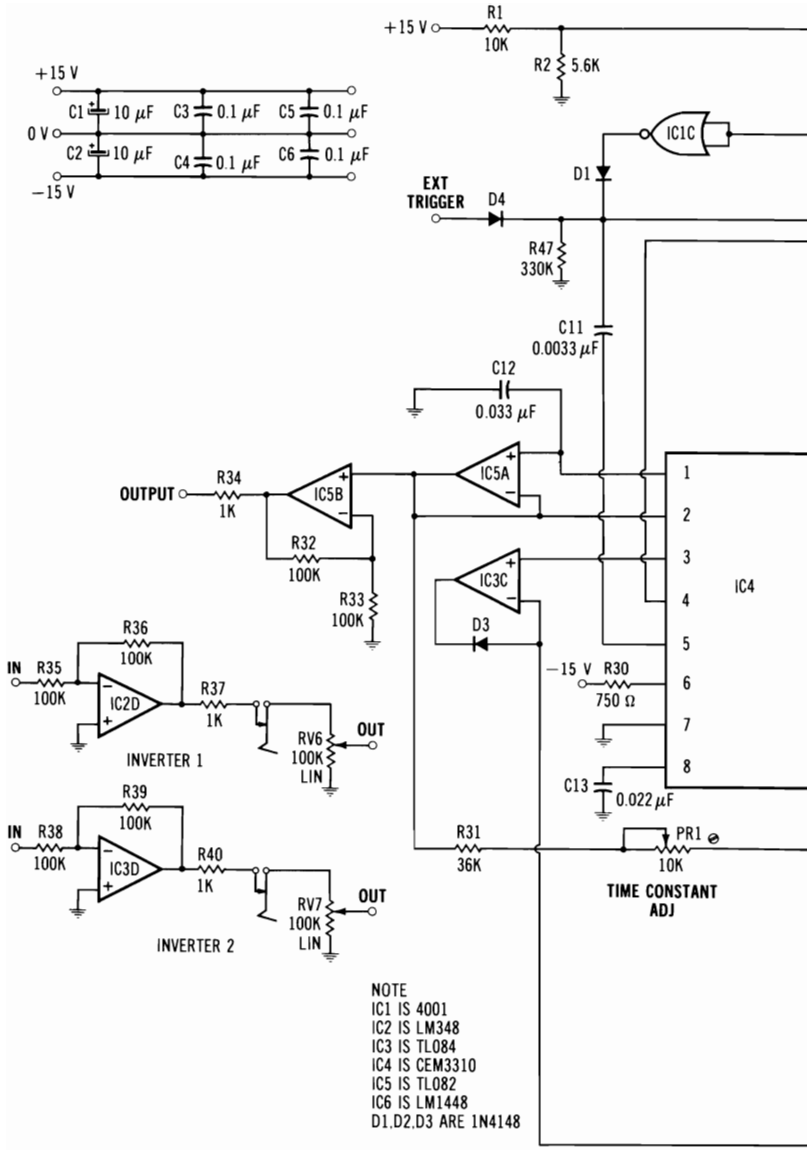
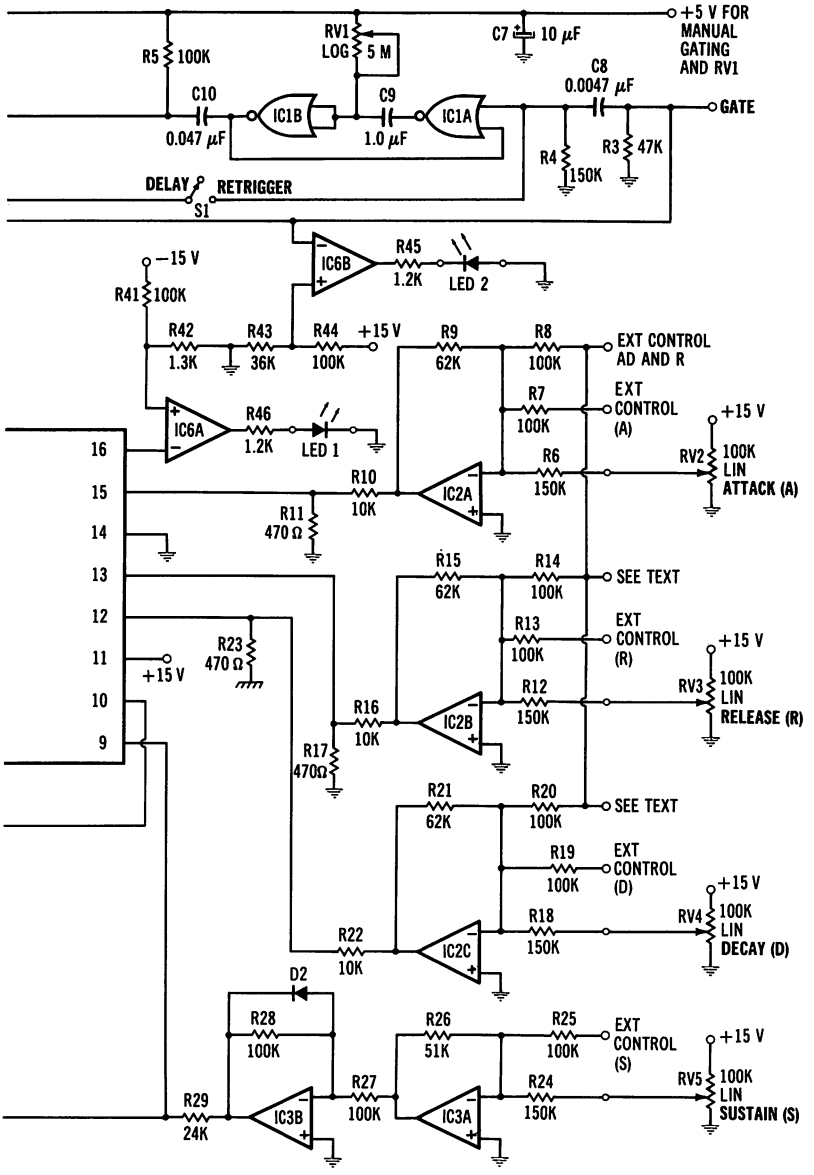



**Fig. 3-16. An envelope generator using the Curtis Electromusic**



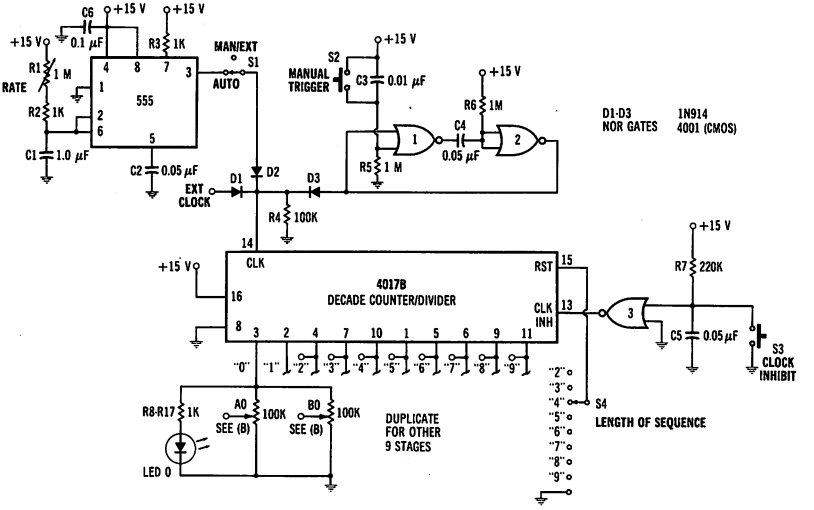

**CEM3310.** *(Courtesy* ETI Magazine *and Digisound, Ltd.)*

undelayed trigger pulse, creating a noticeable delay in the output envelope contour. It may also be desirable to use a separate trigger input to allow retriggering from the keyboard. This is the purpose of diode D4.

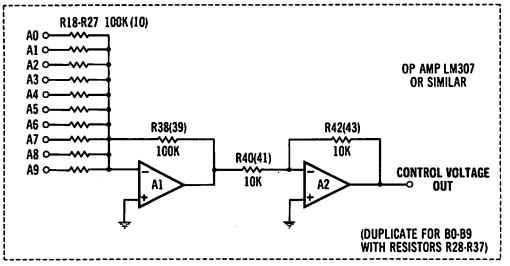
### Sequencers

A sequencer is basically a circuit that generates preset control voltages in a desired sequence. The complexity of sequencers varies greatly. The rate at which the sequencers "step" from one control voltage to the next sequential voltage (the scan rate) can be controlled by an oscillator or an external trigger. The number of different control voltages generated is up to the designer. Individual sequence *times* can also be preset with some designs. In simple designs all the sequence times are equal. Sequencer control voltage data can be read from potentiometers or a digital memory.

Fig. 3–17 shows a simple sequencer using a CMOS 4017B decade counter/divider. Each time a clock pulse occurs on pin 14, the counter in the 4017 is incremented. This count is then decoded internally and, as a result, one of the 10 outputs (0–9) goes to a logic 1. All of the other outputs go to a logic 0. The 555 in this circuit is used as an oscillator whose rate is controlled by R1. Other clock circuits can be used. Switch S1 prevents the oscillator from clocking the 4017, and it allows the use of either an external clock or the manual trigger circuit. In the manual trigger circuit, NOR gates 1 and 2 are configured as a monostable. When S2 is closed this circuit will output a pulse that will clock the counter one step. Pin 13 of the 4017B is the clock inhibit pin. A logic 1 on this pin will inhibit the counter regardless of the clock input status. When this input goes to a logic 0, the counter will continue counting where it left off. The circuitry associated with NOR gate 3 debounces the inhibit switch. A logic 1 on the reset pin (pin 15) will cause the counter to reset to zero. If this pin is connected to an output pin, the counter will count up to the number represented by that pin, reset, and then start counting from zero again. This is the function of S4. If a full sequence (10 states) is desired, pin 15 must be grounded. In addition to S4, the outputs are connected to two 100-kΩ controls and an LED circuit. The LEDs will light as the counter is sequenced. Each divider output also drives two 100-kΩ potentiometers. By adjusting these potentiometers, the user can "pick




(A) Sequencer circuit.




(B) Control voltage circuit.

**Fig. 3-17. A 10-step sequencer.**

off" any voltage between 0 and about 10 V. The wiper voltages are summed with 100-kΩ input resistors and an op amp (A1). Two independent control voltage circuits (A and B) are shown in this figure. One of this control voltage "channels" (A or B) could be used to control an external, voltage controlled, low-frequency oscillator (vclfo). The output of this could be used to clock the sequencer. This could allow variable, individual, sequence times because the frequency of the oscillator would vary with the varying sequencer control voltage output.

Another sequencer design uses a series of monostables configured in a loop. Each monostable triggers the next in the loop. The sequence times are individually set with potentiometers. Fig. 3–18 shows one stage of such a sequence, using the 555 timer.[7] Resistor R1, S1, and capacitor C1 cause the circuit power to be applied slowly, allowing the timers to initially have low outputs. Switch S2 (normally in the RUN position) will initiate the sequencer if it is momentarily grounded. Attention must be paid to proper power supply bypassing with capacitors, since large voltage spikes are created by the 555 timers and can cause unwanted retriggering. CMOS versions of the 555 (Intersil 7555) are less of a problem in this regard.

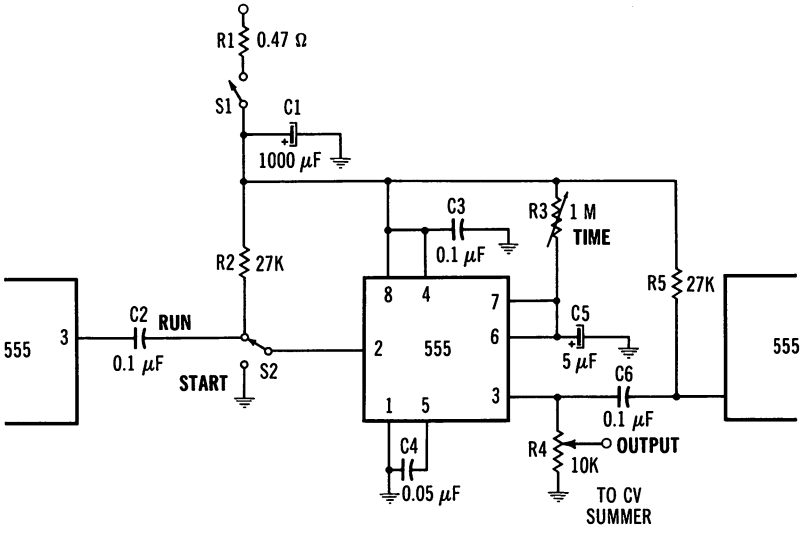



**Fig. 3-18. A sequencer stage using the 555 timer.**

## Noise Sources

Noise sources generate a spectrum of frequencies at random (or appearingly random) intervals. The majority of noise sources are in one of three groups: *white noise, pink noise,* and *low-frequency random voltages.*

White noise has a flat spectral density (all frequencies have equal amplitudes). The interstation hissing you may hear when tuning between fm stations on your stereo is much like white

noise. Pink noise is low-pass filtered white noise, where a note in a higher octave has an amplitude that is 0.707 less than the same note in the next lower octave (3 dB per octave). Low-frequency random voltages are obtained by low-pass filtering the pink noise with a filter with a cutoff frequency of less than 10 Hz.

The majority of noise sources rely on the noise generated by a reverse-biased semiconductor junction. Another method uses digital shift registers. Such a circuit is called a *pseudo-random sequence generator* (prsg). The noise and output level of such a circuit is uniform, but the sequence generated actually repeats at certain intervals.

Fig. 3–19 shows a noise source using a semiconductor junction.[8] Transistor Q1 can be any npn transistor. In fact, what you are looking for here is the noisiest transistor you can find! The noise from this transistor is small in amplitude and is amplified by op amps A1 and A2 for a +5- to −5-volt output. Depending on the transistor, R5 or R6 may have to be changed in order to obtain this output level. Op amp A3 is a low-pass filter with a

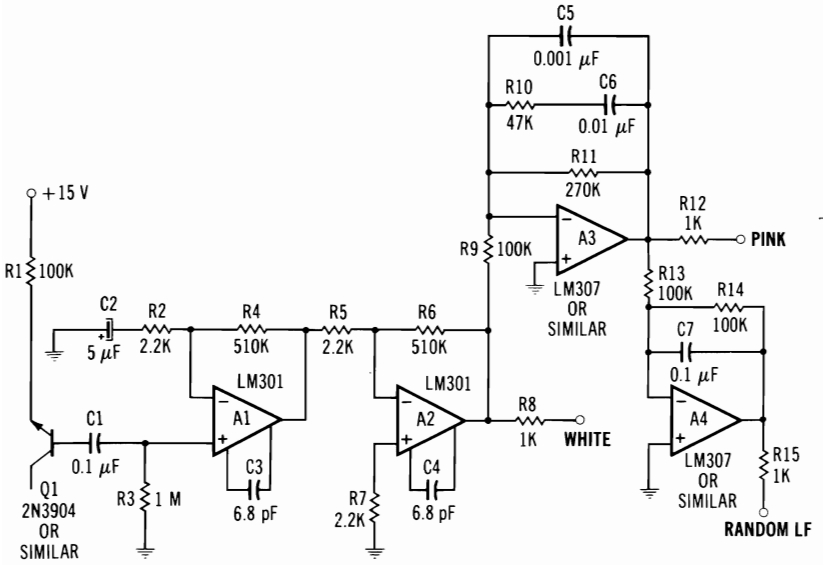



**Fig. 3-19. A noise source using a semiconductor junction.**
*(Courtesy* Electronotes*)*

3-dB/octave roll-off providing pink noise. Op amp A4 is another low-pass filter with a cutoff frequency of about 10 Hz which generates the random low-frequency signal. It should be noted that levels in this circuit will probably have to be trimmed, as the output of Q1 will vary transistor to transistor.

Fig. 3–20 shows a white-noise source using the pseudo-random generator technique. This circuit is used in the Maplin 3800 and 5600 series synthesizers.[9] The four NOR gates are configured as a 35-kHz oscillator to clock the 18-stage shift register IC1. The white noise output is a result of gating (the three EOR gates) the outputs of the 5th, 9th, and 18th stages of the shift register. The white noise is also fed back into the D input of the shift register. Resistor R1 and C1 ensure that the system will start. The sequence output of this circuit will repeat every few seconds but for most applications appears random.

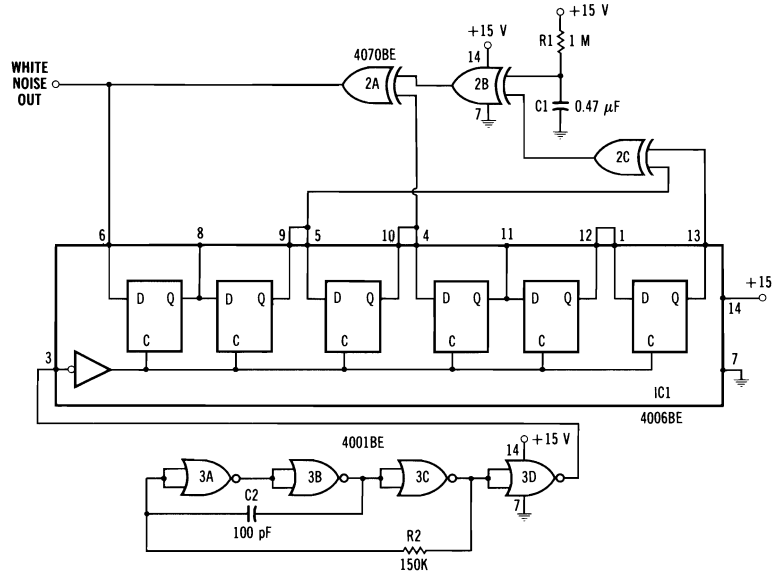



**Fig. 3-20. A white-noise generator using pseudo-random techniques.**
*(Courtesy Maplin Electronic Supplies)*

Fig. 3–21 shows a white-noise source using the National Semiconductor MM5837 IC. This IC is a 17-stage prsg designed especially for white-noise generation. It has an internal clock

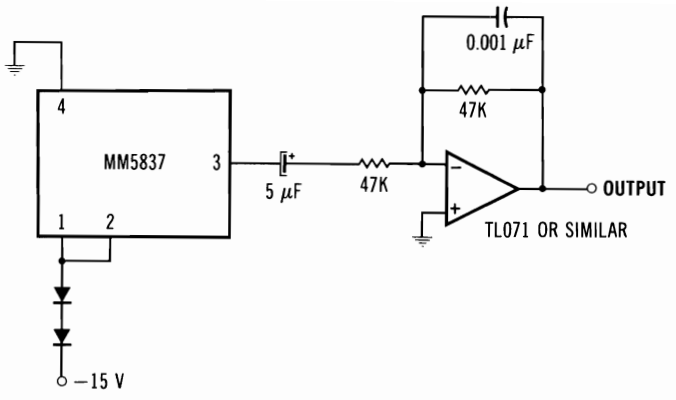



**Fig. 3-21. A white-noise generator using the MM5837.**

frequency of 130 Hz. The white-noise sequence repeats every second. This is slightly audible and puts some limitations on its applications. The previous circuits are less prone to this problem.

## Low-Frequency Oscillators

Low-frequency oscillators (lfo's) generate low-frequency periodic waveforms. Most lfo designs are very simple, consisting of a two op-amp integrator-comparator combination. Such a circuit is shown in Fig. 3–22.[11] Op amp A2 is an integrator whose output rises towards the voltage level set at frequency control R13. The output of A2 rises towards this level until it reaches the upper threshold voltage of the Schmitt trigger (A3). Op amp A3 then changes state and A2 integrates towards the new voltage on R13. Op amp A3 changes states again when the output of A2 reaches the lower threshold voltage of the Schmitt trigger. The threshold voltage of A3 is set by the ratio of R9 to R10. This ratio also determines the amplitude of the triangle-wave output. Typically, the oscillator will have a 100-to-1 frequency variation with the adjustment of R13. Capacitor C1 determines the overall frequency range. Resistors R1 and R2 and diodes D1 and D2 convert the triangle wave to a sine wave. Trimmer R2 adjusts the level of the triangle wave appearing across D1 and D2. These diodes round off the peaks of the triangle wave, causing a sine wave to be generated. Op amp A1 and its associated resistors amplify the voltage across the diodes to +/−5 V.

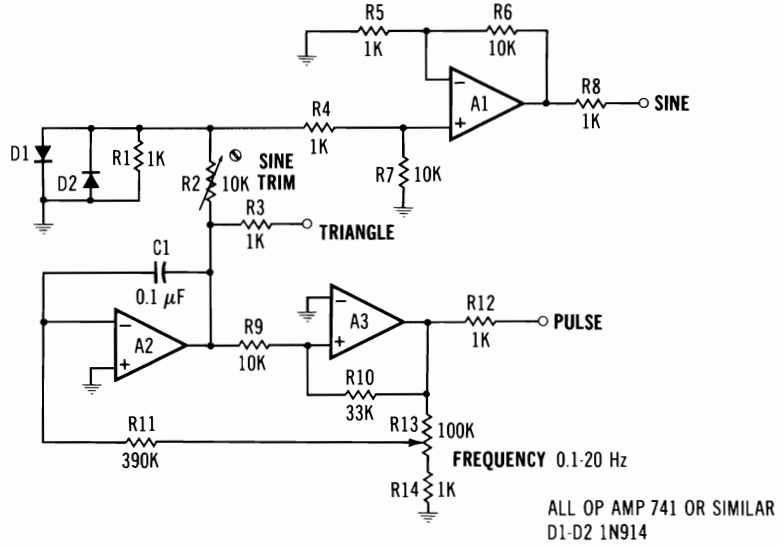



**Fig. 3-22. A simple lfo.** *(Courtesy* CFR Technotes*)*

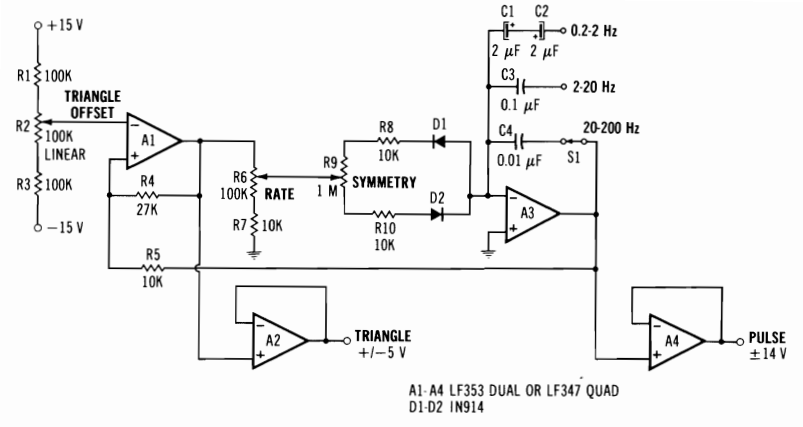
Fig. 3–23 shows another lfo based on these same principles.[12] This circuit, however, has a variable offset control (R2) to raise or lower the triangle waveform and also a symmetry control (R9) to adjust the symmetry of the triangle waveform. Symmetry can be adjusted so that a negative sawtooth, a triangle, or a positive sawtooth can be generated. Simultaneously, this control varies the pulse width output of A3 from 10 to 90 percent. Buffers are provided on the outputs (A2 and A4) to isolate the load from the oscillator circuit. Switch S1 switches between various integrator capacitors for different frequency ranges.

## CONTROL VOLTAGE PROCESSORS

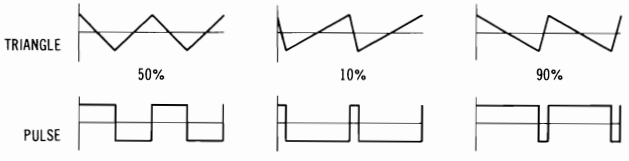
### Sample and Hold Circuits

A sample and hold circuit samples a voltage from an input waveform in response to a clock or trigger pulse. The sample and hold then stores this sampled voltage (in a capacitor) until the next sample command occurs. The effect of a sample and hold on an input signal is shown in Fig. 3–24.

Fig. 3–25 shows a sample and hold circuit. The input signal is buffered by A1. FET Q1 functions as an analog switch, pass-




(A) Circuit.




(B) Effect of symmetry control.

**Fig. 3-23. A lfo with variable triangle offset and symmetry.**
*(Courtesy* Electronotes*)*

ing the analog signal voltage on to storage capacitor C1 when a sample pulse is applied to the gate of the FET. The sample pulse can be derived from an internal oscillator or from an external source. Op amp A4 acts as an inverting comparator. Its output goes to −15 V when its input voltage rises above ground. Diode D3 and R10 convert the +/−15-volt output of A4 to 0–15 volts. Capacitor C5 and R11 convert a *negative transition* (+15 to 0 V) from A4 to a *negative pulse.* The 555 timer (IC1) can act as either an oscillator or monostable multivibrator, depending on the setting of switch S1. If S1 is in the EXT CLOCK position, a negative pulse out of C5 and R11 will trigger the 555, and a pulse with a duration determined by the combination of R12 and C3 will be generated. If S1 is put in the AUTO position IC1 will act as an astable (oscillator) with a frequency determined by R6, R7, and C4. The pulse width remains constant as deter-

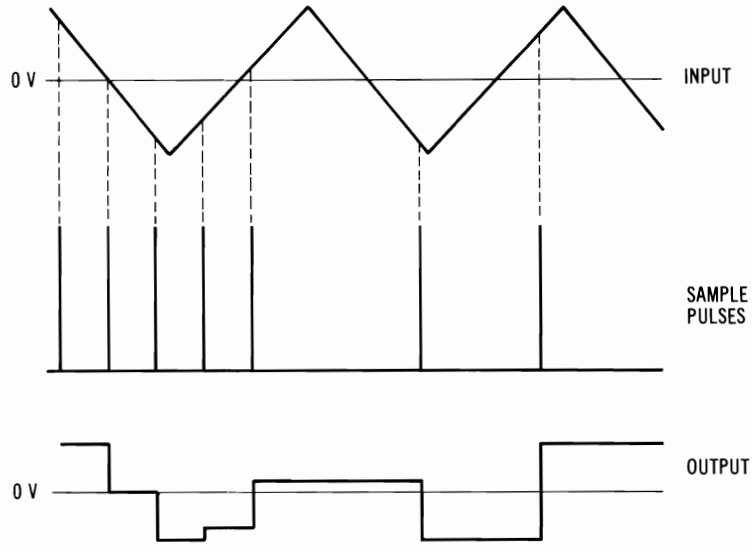



**Fig. 3-24. The effect of a sample and hold on an input signal.**

mined by R12 and C3. Pin 3 is the output of IC1. This 0- to 15-V level is converted to +/−15 V by A3. A +15-V pulse will be blocked by D1 and the output of A1 will pass through R2 to the gate of Q1. This will turn on Q1 and pass the analog signal to storage capacitor C1 and buffer A2. A −15-V level out of IC1 will turn on D1 and the gate voltage will be approximately −14.3 V. This turns Q1 off. Therefore, when an external clock input is used, each time the external clock input rises above ground the input signal will be sampled for a duration equal to the 555 monostable multivibrator output pulse period. When in the AUTO mode, the input signal will be sampled for a duration equal to the 555 pulse period and at a rate set by the rate control (R6).

The on resistance of Q1 and the capacitance of C1 form a time constant that dictates the time required for accurate sample voltage acquisition (by C1). If the sample period (set by R12 and C3) is not long enough, the capacitor will not have enough time to charge up to the level of the input voltage. A smaller value of C1 will remedy this, but the capacitor will be discharged faster by the input impedance of A2. Increasing the sample time period would help, but it will also lower the maximum usable sample frequency.

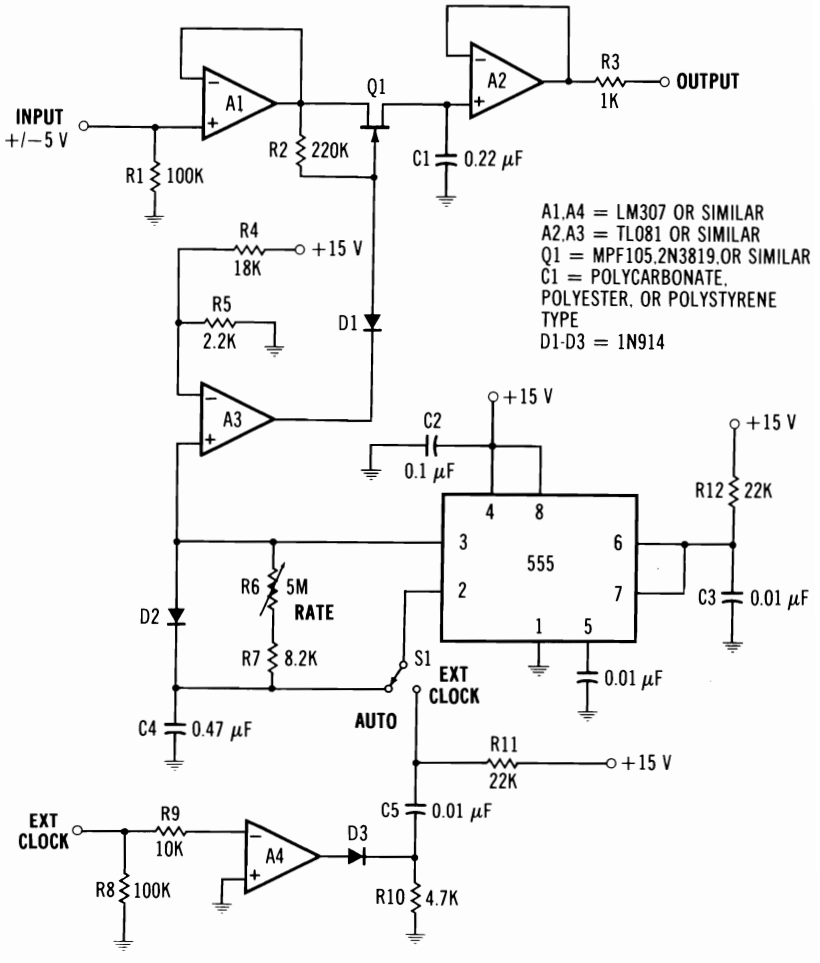



**Fig. 3-25. A sample and hold circuit.**

A bi-FET op amp is used for A2 because of its high input impedance characteristics (less drain on C1:less droop). A polyester, polycarbonate, or polystyrene film capacitor is recommended for C1. Other dielectrics introduce voltage errors due to a dielectric polarization phenomena and also have higher leakage characteristics. A pc foil guard trace leading from the output of A2 and encircling Q1, C1, and "+" input of A2 is recommended to reduce leakage paths surrounding C1.

The 4016 CMOS quad analog spst switch can be used in sample and hold circuits, as shown in Fig. 3–26. The analog signal to be sampled must be within the 4016 power supply limits. The 4016 has a typical on resistance of 300 ohms, but this will vary with the input signal polarity. Other CMOS switches and multiplexers have lower, more consistent on resistances but may have higher droop rates due to higher internal leakage currents.

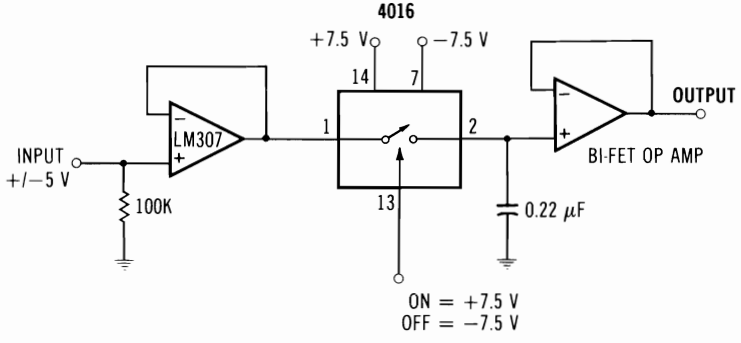
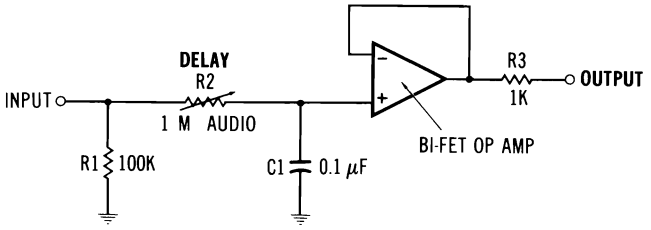



**Fig. 3-26. A sample and hold circuit using a CMOS 4016 switch.**

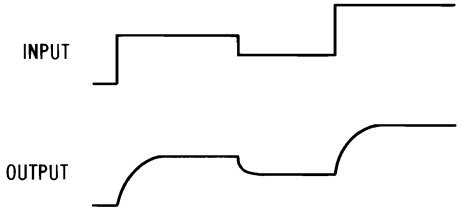
## Slew Limiters

Slew limiters lengthen the rise and fall times of an input waveform. The portamento circuit of a keyboard interface is a slew limiter. Such a circuit is shown in Fig. 3–27A. The time constant of the circuit is determined by the choice of C1 and the setting of R2.

Fig. 3–28 shows a *linear* slew limiting circuit. The heart of the circuit is the integrator formed by R2, R3, C1, and A2. The voltage across capacitor C1 (and thus the output) will be a linear ramp because the capacitor will be charged and discharged at a constant rate (current). Op amp A1 acts as a comparator. Its output normally would be either high or low (+/−14 V). Resistors R2 and R3 determine the charging current from the output voltage of A1 (the current in the feedback path of A2 is equal to the current through R2 and R3). The output of A2 is fed back into comparator A1. The output of A1 corrects for any voltage difference between the inverting (−) input of A1 and the output of A2. If the input level remains constant, A1 output oscillates at a




(A) Circuit.



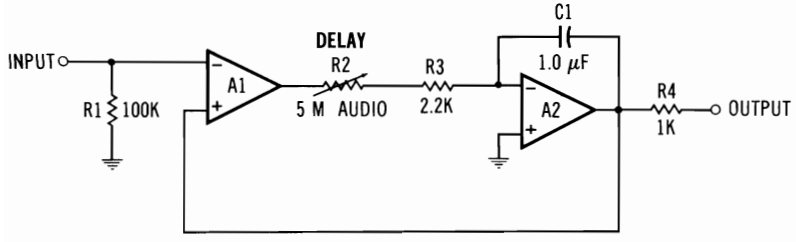

(B) Waveforms.

**Fig. 3-27. An exponential slew limiting circuit.**

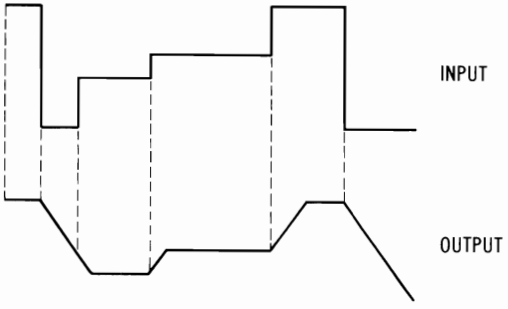
very high frequency and the output of A2 is a constant dc level identical with the input.

## Trigger and Gate Extractors

*Gate and trigger extractors* derive timing signals from an input waveform. Some of the previous keyboard interface and envelope generator circuits contained these circuits. The basic gate extractor circuit is the comparator circuit in Fig. 3–29. As the input voltage across resistor R3 rises above the voltage on the inverting input of op amp A1 (set by divider resistors R1 and R2) the output of A1 will shift from a low saturation level to a high saturation level. The saturation level of the op amp will depend on the supply voltages and the actual type of IC used. The maximum output voltages for op amps, for typical supply voltages, are given in the op-amp data sheets. Diode D1 and resistor R4 limit the output to 0–15 volts in this circuit. Sometimes the circuit that requires a gate signal has an input that is ground referenced. Since the output of this circuit is between 0 and 15 volts, it may not properly gate some circuitry, because it does not drop below ground. Resistor R5 and zener diode D2

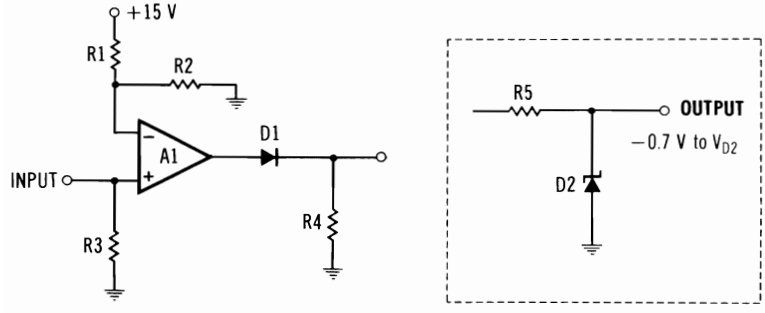



(A) Circuit.




(B) Waveforms.

**Fig. 3-28. A linear slew limiting circuit.**




(A) Circuit.

(B) Alternate output circuit.

**Fig. 3-29. A comparator used for gate extraction.**

can be used in place of diode D1 and resistor R4 to provide an output that rises from −0.7 volt to the zener voltage of the zener diode.

If the input to the circuit of Fig. 3–29 is unstable or has noise imposed on it, the comparator may change states several times, as shown in Fig. 3–30. This is not very desirable. *Hysteresis* is added to allow the circuit to "ignore" the noise and jitter of the input signal. Hysteresis is the creation of two voltage thresholds caused by the addition of positive feedback to the circuit. This is shown in Fig. 3–31. Resistors R3 and R4 form a voltage divider between the input voltage and the output (saturation) voltage of the op amp. Resistor R4 adds positive feedback to the circuit. As the value of R4 is increased (or R3 decreased) the amount of positive feedback will decrease and there will be less of a voltage difference between the upper threshold points (less hysteresis).

A similar circuit designed with the 4050 CMOS buffer is shown in Fig. 3–32. This circuit is commonly termed a *Schmitt trigger*. The threshold point of the CMOS 4050 is normally

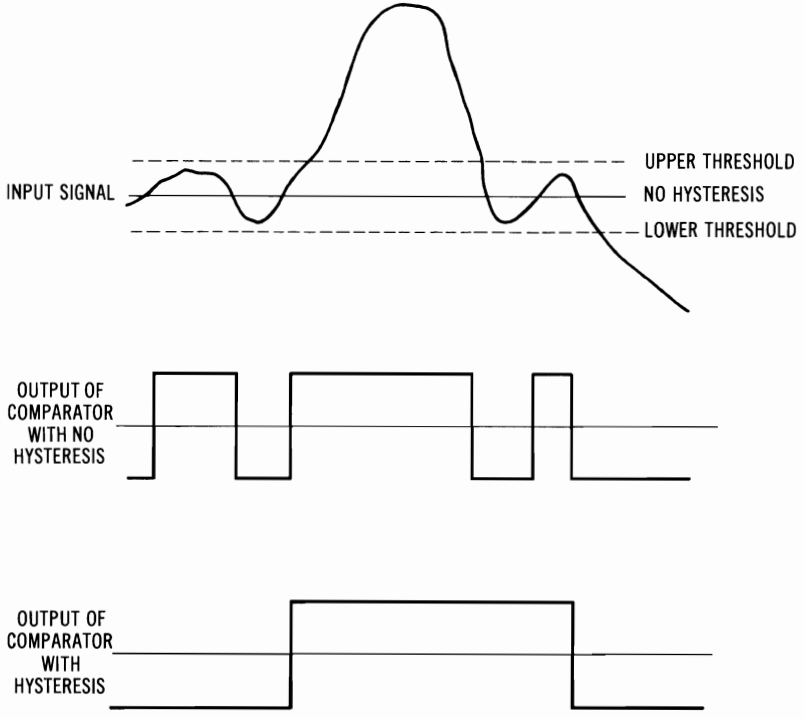



**Fig. 3-30. Outputs of a comparator with and without hysteresis.**

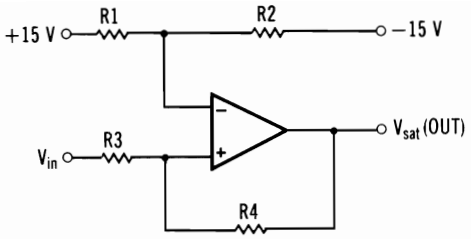



**Fig. 3-31. A comparator with hysteresis.**

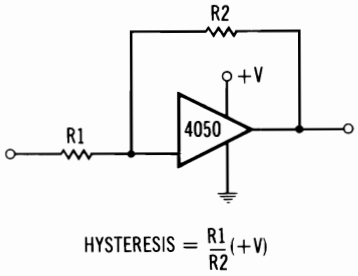
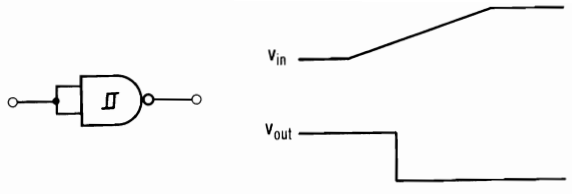



**Fig. 3-32. A Schmitt trigger using the CMOS 4050 buffer.**

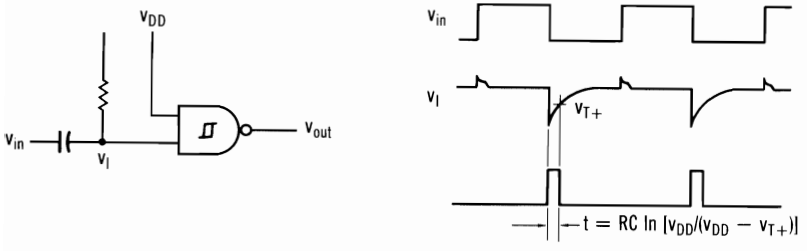
close to one-half of the supply voltage. Positive feedback is added by resistor R2.

The CMOS 4093 is a dual two-input NAND gate Schmitt trigger that has a typical 2.7-V hysteresis for a 15-V power supply voltage. Fig. 3–33 shows the 4093 used in signal conditioning and trigger circuits.

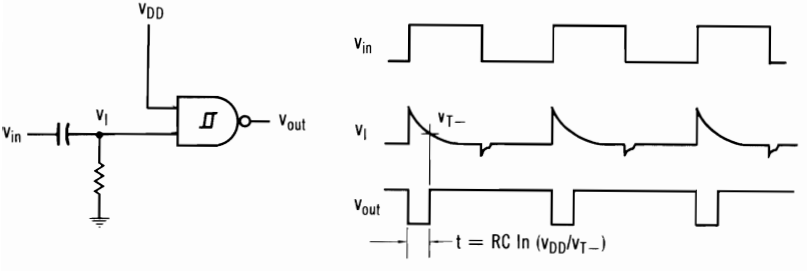
An op-amp differentiator circuit may be used to help generate a trigger if an input voltage changes in an abrupt step. This type of circuit was used in the monophonic keyboard interface of Fig. 3–3. The differentiator is actually a high-gain inverting ac amplifier. An increase in the keyboard control voltage would cause a negative pulse out of the differentiator and trigger the 555 monostable. A decrease in the keyboard control voltage will cause a positive pulse out of the differentiator. This would not normally trigger the 555. However, contact bounce within the keyboard can cause a negative pulse to be generated by the differentiator, triggering the 555. For input signals with "clean" transitions the circuit will only generate trigger pulses for increases in the control voltage. The circuit of Fig. 3–34 will generate a trigger pulse anytime the input voltage changes from a relatively constant fixed voltage level. You may wish to experi-




(A) Schmitt trigger operation.



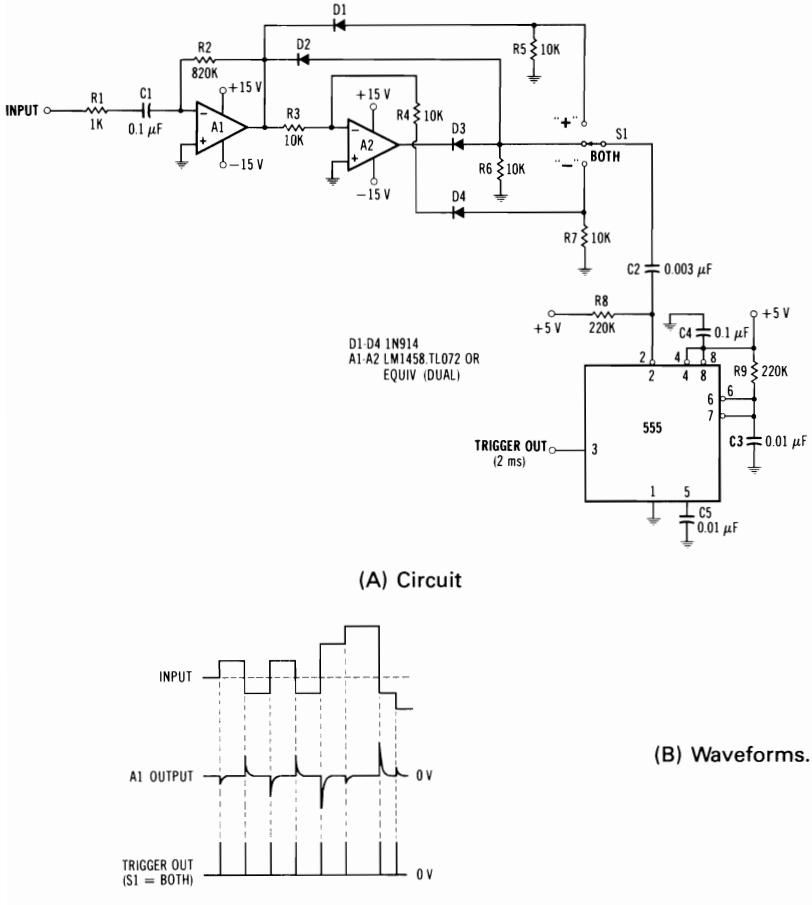

(B) Negative-edge triggered.




(C) Positive-edge triggered.

**Fig. 3-33. Signal conditioning and trigger circuits using the CMOS 4093 Schmitt trigger.** *(Courtesy National Semiconductor Corp.)*

ment with the component values in the differentiator circuit to increase or decrease its sensitivity. Increasing resistor R1 or decreasing resistor R2 will reduce the gain of the circuit. Increasing the value of C1 will allow inputs with slower rise and fall times to generate trigger pulses. The 555 timer IC is operated at 5 V mainly to reduce power supply loading (3 mA at 5 V vs. 10 mA at 15 V) and to eliminate voltage spikes on the ±15-V power supply. The CMOS version of the 555 can be used at 15 V if desired. Note that this circuit has a very low input impedance.




(A) Circuit




(B) Waveforms.

**Fig. 3-34. A trigger extractor circuit.**

A buffer may be necessary for some applications. If you wish the trigger to be delayed slightly, increase the pulse width out of the 555 by changing resistor R9 and/or capacitor C3. Then feed the output into another 555 monostable circuit as in Fig. 3–3.

## Envelope Followers

An envelope follower is basically an ac-to-dc converter. It generates a dc level that corresponds to the average peak amplitude of an ac input signal. The input signal is first full-

wave rectified and then filtered to obtain a relatively smooth dc output. This type of circuit is used to obtain an amplitude "envelope" of an input signal. The output can then be used as a control voltage for other modules such as a voltage controlled filter or voltage controlled amplifier.

An envelope follower circuit is shown in Fig. 3–35. It originally appeared in *Electronotes.*[13] Op amps A1 and A2 form a precision full-wave rectifier. The output of half-wave rectifier A1 is summed with the input signal to obtain a full-wave output. For negative input signals the output of A1 is 0 V and the input signal flows through resistor R4 and R3 to op amp A2. For positive input signals the signal will flow through half-wave rectifier A1 and resistors R4 and R3 to op amp A2. Resistor R5 sets the gain of the circuit. Capacitor C2 filters (integrates) the full-wave peaks to provide a stable output from op amp A2. If the value of capacitor C2 is too small, the output of A2 will vary slightly, or

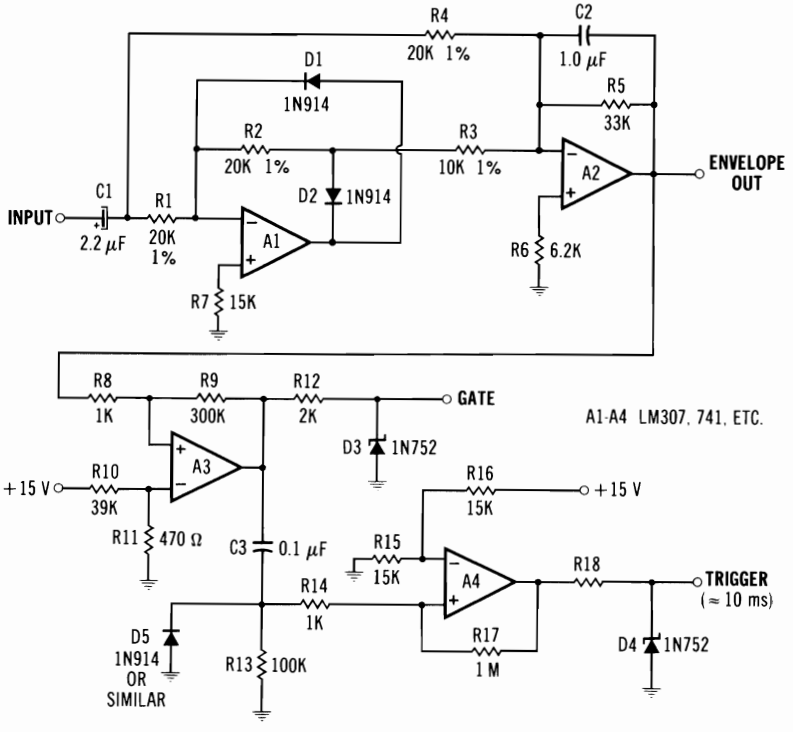



**Fig. 3-35. An envelope follower.**

ripple. Op amp A3 is a comparator with hysteresis and generates a gate signal if the input rises above 500 mV peak to peak. Op amp A4 generates a trigger signal when the gate signal occurs. The type of op amp used in this circuit is not critical. One-percent resistors are used in the rectifier circuit for precision. For some uses, 5-percent resistors may be fine. It may be necessary to experiment with values for capacitor C3 and/or resistor R13 for proper trigger generation.

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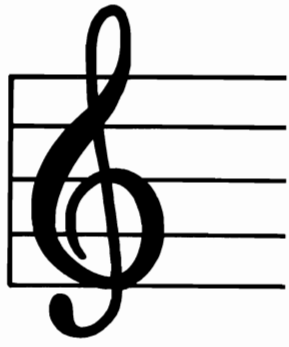
*For information on publications about synthesizers see Appendix A.

# VOLTAGE CONTROLLED OSCILLATORS (VCO'S)



# CHAPTER 4

Voltage controlled oscillators (vco's) generate one or more periodic waveforms whose frequency is a function of an input control voltage. Most vco's in electronic music circuits contain an *exponential converter* that converts a linear input control voltage (such as a keyboard output) to an exponential current. This current is used to control a *current controlled oscillator* that has a large dynamic range. The output of the oscillator is used to drive several *waveform conversion/generation* circuits. These circuits provide the typical triangle, sawtooth, sine, and pulse waveform outputs (Fig. 4–1).

The vco is the most important and easily criticized circuit in a synthesizer. A vco must have a large frequency (dynamic) range, an accurate 1-volt-per-octave response through its range, and should have an output frequency that is independent of ambient temperature. Most of the burden of meeting these criteria falls on the performance of the exponential converter.

## THE EXPONENTIAL CONVERTER

The process of converting a linear voltage to an exponential current is based on the fact that the collector current of a transistor is an exponential function of its base-emitter voltage ($V_{BE}$). The use of a single transistor, however, is undesirable because its emitter saturation current ($I_{ES}$) doubles for every 10°C. Therefore a second and identical transistor is added to cancel out this temperature effect. The best result is achieved if these

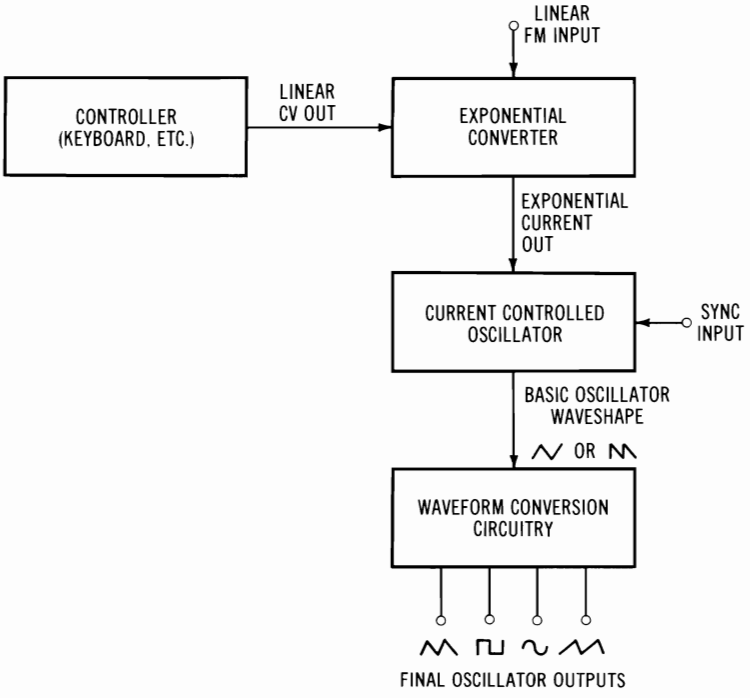



**Fig. 4-1. Functional diagram of a voltage controlled oscillator.**

transistors are packaged as a dual transistor, part of an array, or at least a matched pair of transistors that are epoxied together.

Fig. 4–2 shows such a circuit in its practical form.[1] Op amp Al and resistors R1–R6 provide control voltage ranging and scaling. These components are chosen so that for a 1-volt-per-octave response, a 1-volt increase in the input control voltage causes an 18-mV increase on the base of transistor Q1. Trimmer R5 adjusts the converter for a 1-volt-per-octave response.

The control range is set by the reference current ($I_{ref}$) which goes to the collector of Q1. This will be the output current of transistor Q2 when the input control voltage is 0 volts. The value of $I_{ref}$ is usually set for 10 $\mu$A or more to negate any effect the bias current of op amp A2 may have on the output current. Resistor R9 limits the maximum current generated by the circuit and therefore sets the high-frequency limit of the oscillator.

The output current of the circuit is given by the following equation:

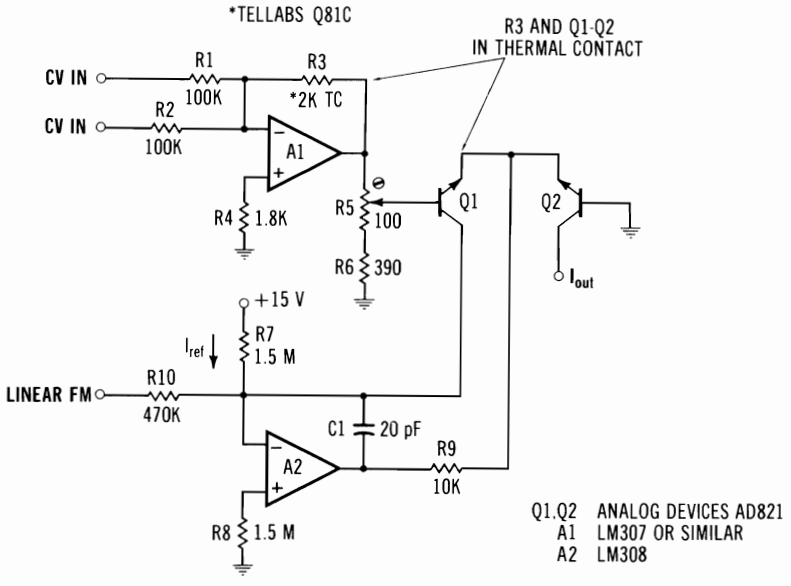



**Fig. 4-2. An exponential converter circuit.**

$$I_{out} = I_{ref} \exp (V_B q/kT)$$

where

$V_B$ = voltage on the base of Q1 in millivolts,
$q$ = charge of a single electron ($1.60219 \times 10^{-19}$ coulomb),
$k$ = Boltzmann's constant ($8.6167 \times 10^{-5}$ electron volts per kelvin),
$T$ = temperature in kelvins.

The temperature-dependent term in the exponential current conversion equation changes the exponent about 0.33 percent per degree Celsius change in temperature. Resistor R3 has a positive temperature coefficient of 3500 ppm/°C and, when placed in contact with Q1 and Q2, will cancel out the temperature term by changing the control voltage output by op amp Al.

An alternate method of eliminating the temperature-dependent term is to use a thermostat to heat the transistors to a temperature above the ambient level. Such a circuit is shown in Fig. 4–3.[2] In this circuit the heater and exponential conversion transistors are part of a CA3045/6 transistor array. The tempera-

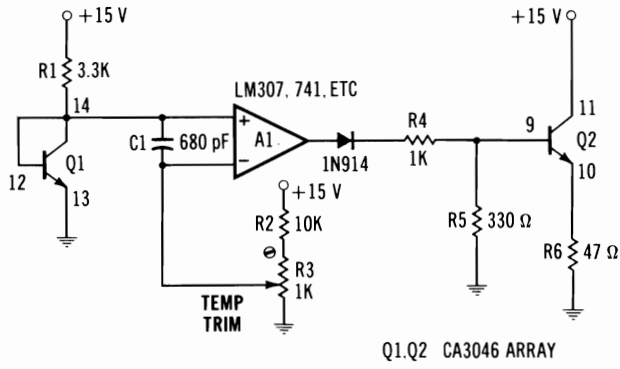



**Fig. 4-3. A thermostat circuit.**

ture of the IC is sensed by diode-connected transistor Q1. It is compared with the thermostat setting of trimpot R3. If the temperature is below the level set by R3, comparator Al will go high and turn on heater transistor Q2. Resistors R4 and R5 limit the maximum collector current to 50 mA—the limit of the IC.

Another problem with transistor-based exponential converter circuits is their bulk emitter resistance. This resistance is insignificant at low frequencies but at high frequencies (higher current) it is high enough to affect the output current and cause the oscillator to go flat. If a portion of the exponential current is inverted and fed back into the converter, the emitter resistance effect is cancelled.

This feedback is done in the circuit of Fig. 4–4.[3] In this circuit the transistors are part of a CA3045/6 transistor array. Since all transistors are on the same piece of silicon, the die, thermal tracking is excellent. An LM308 is used for IC2 for its low input bias current and low input offset voltage drift with temperature. A portion of Q3's emitter current is fed back through R13 to correct for high-frequency tracking error. Temperature-compensation resistor R4 is placed in contact with the CA3046 to provide close tracking. To adjust tracking of this circuit, R15 is first set to its minimum value. The V/OCT trimmer, R6, is adjusted for a 1-volt-per-octave frequency response between two low octaves. After R6 is adjusted, R15 is adjusted for a 1-volt-per-octave response between low and high octaves.

Linear voltage control of the vco frequency is accomplished by adding to, or subtracting from, the reference current ($I_{ref}$) for

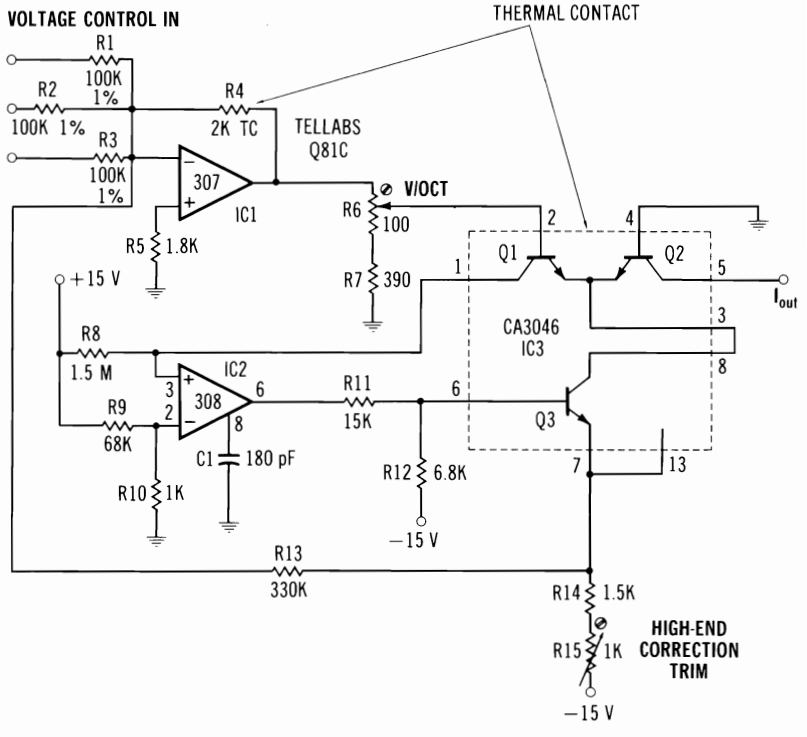
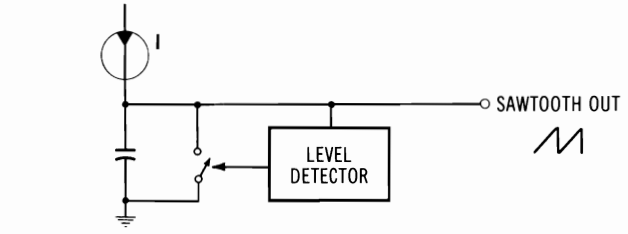



**Fig. 4-4. An exponential converter circuit using a CA3046 transistor array.**

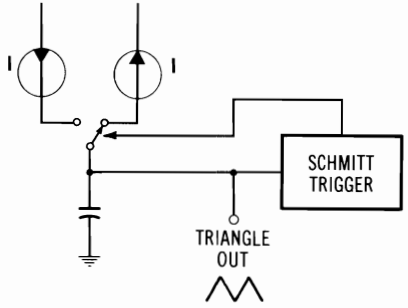
the transistor pair, which flows through Q3. This is the function of resistor R10 in Fig. 4–2.

## THE CURRENT CONTROLLED OSCILLATOR

Two types of current controlled oscillators are commonly used in vco designs. These are diagrammed in Fig. 4–5. The *sawtooth oscillator* (Fig. 4–5A) consists of a current source (exponential converter), a storage capacitor, a level detector, and a switch. The current source charges the storage capacitor up to the threshold voltage of the level detector. At this point the level detector closes the switch, which discharges the storage capacitor. Once the switch is opened, the storage capacitor begins recharging up to the level detector threshold again. *The voltage across the storage capacitor will increase linearly towards the threshold voltage, due to the constant current*




(A) Sawtooth oscillator.




(B) Triangle oscillator.

**Fig. 4-5. Functional diagrams of current controlled oscillators.**

*charging it*. Changing the threshold voltage will change both the frequency and voltage output level of the oscillator. Increasing the charging current will increase the oscillator frequency because the capacitor will charge to the threshold voltage faster.

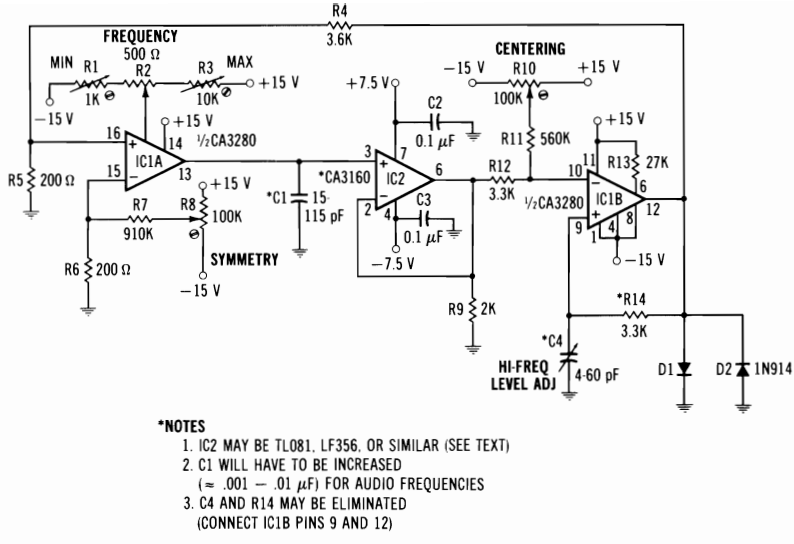
The level detector must be able to detect the threshold voltage very quickly or else it will introduce high-frequency tracking errors. Also, if the on resistance of the discharging switch is too high, there will be an error caused by the time needed to discharge the storage capacitor. After the basic oscillator design has been optimized, some high-frequency error may still exist. This can usually be cancelled out by compensation in the exponential converter circuit. Often both the error caused by the converter bulk emitter resistance and the reset error can be cancelled out simultaneously.

Another current controlled oscillator is the *triangle oscillator*. This type of oscillator (Fig. 4–5B) consists of a storage capacitor, a current reversing switch, and a Schmitt trigger (see Chapter 3). The storage capacitor is first charged up to the upper threshold of the Schmitt trigger. The Schmitt trigger then

changes states, and the polarity of the charging current is reversed. The charge on the storage capacitor will then ramp down until it reaches the lower threshold of the Schmitt trigger. The output frequency of the oscillator is dependent on the charging current and the value of the storage capacitor. The output amplitude is set by the thresholds of the Schmitt trigger.

The device used for the current reversing switch is an *operational transconductance amplifier*, or *ota*. An ota is an op amp with a *current* output, the magnitude of which is a function of the differential input voltage and a bias current ($I_C$). For input voltages of 10 mV or less the op amp operates linearly and $I_C$ will function as a gain control. If the input voltage of the ota is large (more than 1 volt), the input will be saturated and the output will be a current with a polarity of the input voltage and an amplitude equal to the $I_C$ control current. Thus, if a square wave is input to an ota, the output will alternately source and sink a current equal to $I_C$. RCA was the first manufacturer to produce a commercially available ota: the CA3080. Lately, dual ota's have been introduced by several manufacturers. These include the RCA CA3280, the National Semiconductor LM13600, and the Signetics NE5517. These new ota's contain input (linearization) diodes that can be biased to predistort the input signal. The input transistors in an ota already distort the input signal in one direction, and so the two distortions cancel, allowing larger input signals. Linear uses of ota's are covered in Chapters 5 and 6. The linearization diodes in ota's are generally not used in vco circuits, because input saturation is desired.

Fig. 4–6 contains an oscillator circuit using ota's based on a circuit in the RCA CA3280 data sheets.[4] Op amp IC2 buffers the voltage across capacitor C1. This op amp (a CA3160) may be replaced with a TL081 or similar FET input op amp to eliminate the necessity of +/−7.5-volt supplies. Op amp IC1B acts as a threshold detector to alternate direction of current out of current source IC1A. The voltage drop across diodes D1 and D2 is fed to the IC1B noninverting input by resistor R14. Op amp IC1B changes output states whenever the input to pin 10 reaches the threshold level set at pin 9. Note that the frequency of this circuit (monitored at IC2 pin 6) is controlled by the current through pin 3 of ota IC1A. If we apply the output of the exponential converter to this pin, we will have a basic vco. This circuit was intended as a function generator with a large




*NOTES
1. IC2 MAY BE TL081, LF356, OR SIMILAR (SEE TEXT)
2. C1 WILL HAVE TO BE INCREASED
(≈ .001 − .01 μF) FOR AUDIO FREQUENCIES
3. C4 AND R14 MAY BE ELIMINATED
(CONNECT IC1B PINS 9 AND 12)

**Fig. 4-6. A wide-range current controlled oscillator.**

dynamic range (2 Hz to 1 MHz). The value of C1 will have to be increased to optimize the circuit for audio frequencies.

## DISCRETE VCO CIRCUITS

Fig. 4–7 contains a complete vco circuit using a current controlled oscillator circuit similar to the one in Fig. 4–6.[5] The AD821 (Analog Devices, Inc.) is a dual transistor optimized for logarithmic/exponential conversion circuits. Note that in this circuit, pnp transistors are required in the exponential converter circuit to supply current to the CA3080. Also, the linear control voltage is applied to the second transistor (Q2). This allows higher control voltages to correspond to higher frequencies.

Op amps IC4, IC5, and IC6 make up the current controlled oscillator. Resistors R15 and R21 attenuate the output of IC5. This causes the oscillator output (from IC5) to increase above normal to compensate for the attenuation due to these resistors. Resistors R15 and R21 are chosen so that IC5 generates a 10-V (peak-to-peak) signal. The resulting triangle waveform is fed to an ota (IC7). This large signal overdrives the ota input. The current output of the ota is converted to a sine wave voltage by op

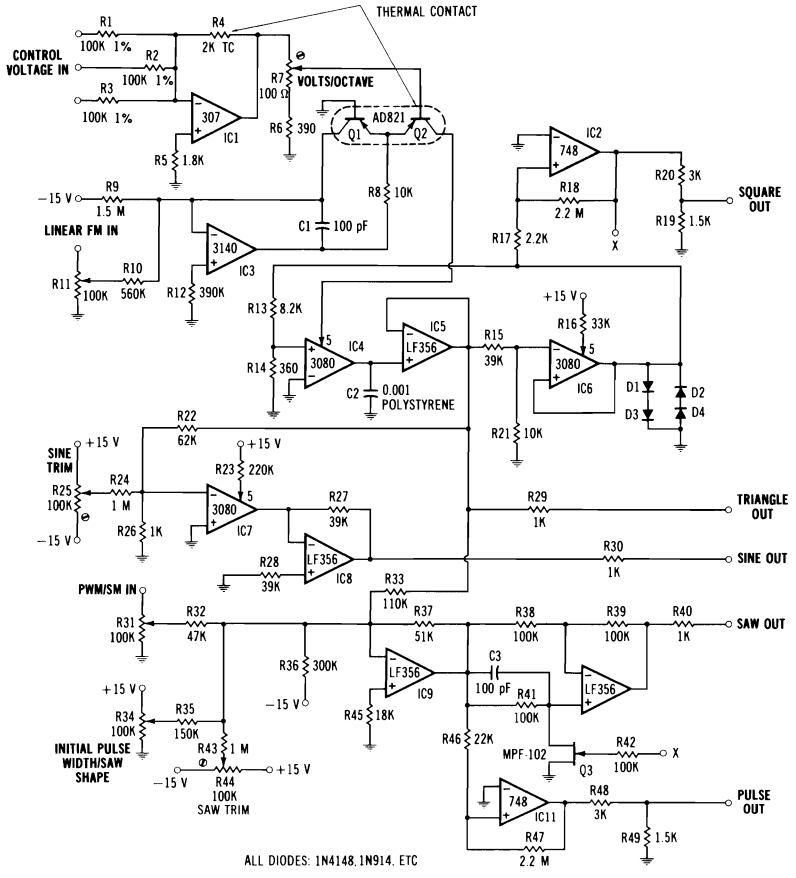



**Fig. 4-7. A vco using a triangle-wave current controlled oscillator.**

amp IC8. The "roundness" of the sine wave adjusted by the setting of trimmer R22. The symmetry of the sine wave is adjusted by R25.

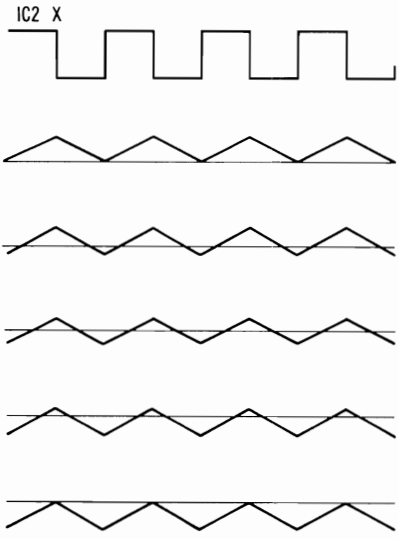
Op amp IC2 acts as a Schmitt trigger and converts the low-level square wave generated by ota IC6 to a high-level square wave. Resistors R19 and R20 attenuate this to 10 V p-p.

The circuitry consisting of IC9, IC10, and IC11 performs both pulse width modulation and sawtooth generation/modulation. Op amp IC9 acts as a summing amplifier. It adds the dc levels from trimmer R44 and INITIAL PULSE WIDTH control R34 to the oscillator triangle waveform and a modulation control voltage

from PWM/SM control R31. When the output of IC9 is fed into a ground-referenced Schmitt trigger, such as IC11, a periodic pulse is output. The duty cycle and pulse width of the pulse will vary as the average dc level of the triangle waveform varies. Op amp IC10 is made to invert the output of IC9 with a switch signal from IC2. If FET Q3 is switched on, IC10 acts as an inverter. If Q3 is off, IC10 is a noninverting unity-gain amplifier. If the output of IC9 is trimmed to 0–5 volts, the output of IC10 will be a +/−5-volt sawtooth waveform. By varying the average dc level of the triangle waveform the output of IC10 will vary from a normal sawtooth to a low-level sawtooth with twice the normal frequency, as shown in Fig. 4–8. Op amp IC11 acts as a zero-crossing Schmitt trigger. It generates a pulse waveform with a duty cycle determined by the dc level of the triangle output of IC9. Resistors R48 and R49 attenuate the output of IC11 to +/−5 V peak to peak.

A vco circuit using a sawtooth current-controlled oscillator is shown in Fig. 4–9.[6] The AD818 is a logarithmic amplifier manufactured by Analog Devices. The exponential conversion circuitry can be replaced with the lower-cost circuit in Fig. 4–4.

Op amps IC2 and IC4 make up a sawtooth oscillator with an

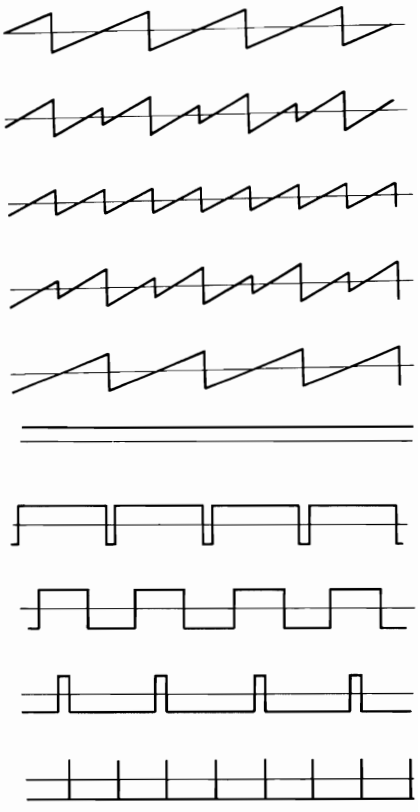



(A) Level-shifted triangle: IC9 output.

**Fig. 4-8. Waveforms for**

output of 0–5 volts. In operation the exponential current from transistor Q2 charges integrator capacitor C1. The voltage output of IC2 rises linearly until it reaches the threshold of comparator IC4. The output of IC4 then switches from −15 V to ground. This enables FET switch Q3 and discharges C1. Capacitor C4 and resistor R12 allow Q3 to fully discharge capacitor C1 by creating an *RC* time delay of the voltage appearing at pin 2 of IC4. Without this delay, IC4 would oscillate at a very high frequency, determined by its internal switching time.

The sync input gives us the ability to reset the sawtooth oscillator (the integrator) with an external pulse. This pulse is usually generated by another vco. Synchronizing oscillators in this



(B) Modulated sawtooth: IC10 output.

(C) Pulse output: IC11

**the circuit of Fig. 4-7.**

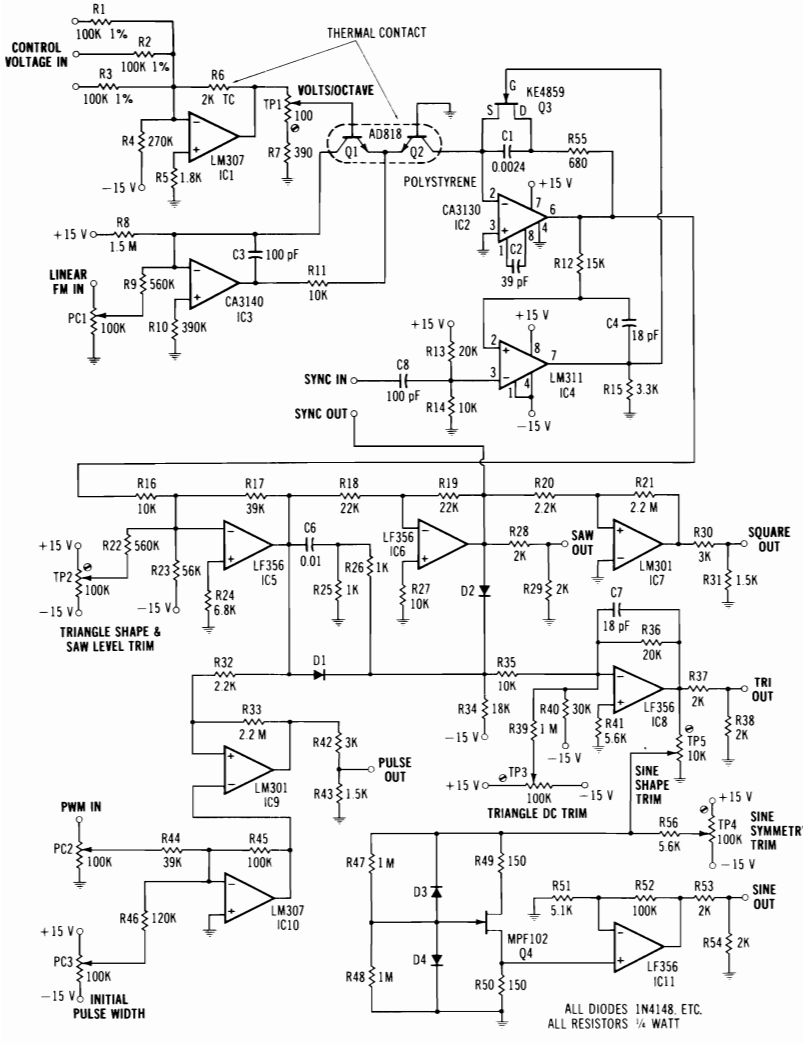



**Fig. 4-9. A vco using a sawtooth current controlled oscillator.**

manner is usually done when the frequencies of two oscillators are set to a specific ratio and precise tracking is desired. The oscillator generating the sync pulse is called the *master* oscillator and the oscillator receiving the sync signal is called the *slave* oscillator. Interesting timbral effects can be heard if the

slave vco is modulated while the master oscillator frequency is held constant.

Resistor R55 in the integrator corrects for high-frequency tracking error caused by the finite switching time of the FET switch. The inclusion of this resistor in the integrator causes the output of the oscillator to reach the threshold point of the comparator sooner, making up for this switching delay. If the value of this resistor is increased, it can also correct for the bulk emitter resistance problem in the exponential converter. This resistor generates a similar linear term that *only* becomes apparent at high frequencies. The value of this resistor may have to be adjusted for best tracking.

Op amps IC5, IC6, and IC8 form a sawtooth to triangle-wave converter. Op amp IC5 amplifies the sawtooth output of the integrator (IC2) to +/−10 V. Inverter IC6 provides an inverted sawtooth output signal to attenuator resistors R28 and R29. Diodes D1 and D2 sum the positive ramp of the sawtooth waveform from op amp IC5 and the negative ramp from IC6, resulting in a triangle wave of 0–10 volts. Op amp IC8 amplifies and shifts the level of this signal. Capacitor C6 and resistor R26 (on the output of IC5) compensate for "glitches" that occur in the triangle waveform due to the drops across diodes D1 and D2, by introducing a similar glitch of reverse polarity. Capacitor C7 (in the feedback of IC8) filters out or reduces any residual glitch present. The output of IC6 can be used to sync similar oscillator circuits. Op amp IC9 functions as a Schmitt trigger, providing a pulse whose width is determined by a reference voltage from op amp IC10.

Sine wave conversion is achieved by FET Q4 and op amp IC11. The resistance of Q4 will vary with the voltage appearing at its gate. As the signal level of the triangle waveform increases, Q4 attenuates or "rounds off" the peaks. Thus the signal across resistor R50 resembles a sine wave. This signal is amplified and buffered by op amp IC11. Trimmer resistors TP4 and TP5 adjust the symmetry and "roundness" of this sine wave.

## ADDITIONAL WAVESHAPING CIRCUITS

The last two vco circuits (Figs.4–8 and 4–9) included various types of *waveshaping* circuits. The following are additional examples of waveshaping methods used in vco circuits.

It is possible to perform a triangle to sine-wave conversion using piecewise linear approximation techniques (Fig. 4–10). The diodes in this design each begin to conduct at different input signal amplitudes. As each diode begins to conduct, it shorts a portion of the input signal to ground through one or more resistors. This has an overall effect of rounding the peaks of the input triangle waveform to form a sine wave. Capacitor C1 blocks any dc offset in the input waveform. It may be left out if the input signal doesn't contain an offset, or if an offset trimmer is added to IC1A.

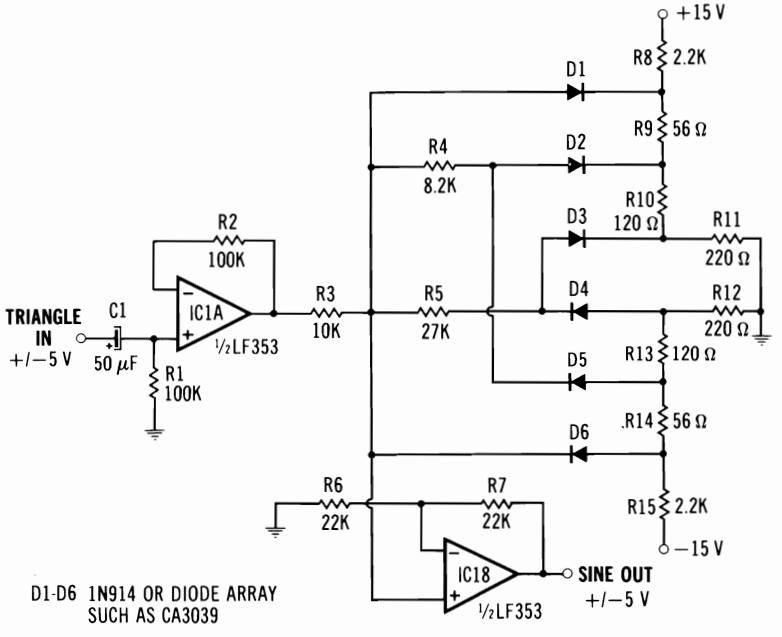



**Fig. 4-10. A triangle-wave to sine-wave conversion circuit using piecewise linear approximation techniques.**

Fig. 4–11 contains a triangle to sine-wave converter based on a published circuit.[7] This circuit is similar to the CA3080 circuit in Fig. 4–7, in that a triangle wave is used to overdrive a differential amplifier input to create a sine wave. The output currents of the two ota's are summed together and are converted to a voltage by op amp IC2. Resistor R13 determines the amplitude of the resulting sine wave. The roundness of the sine wave is

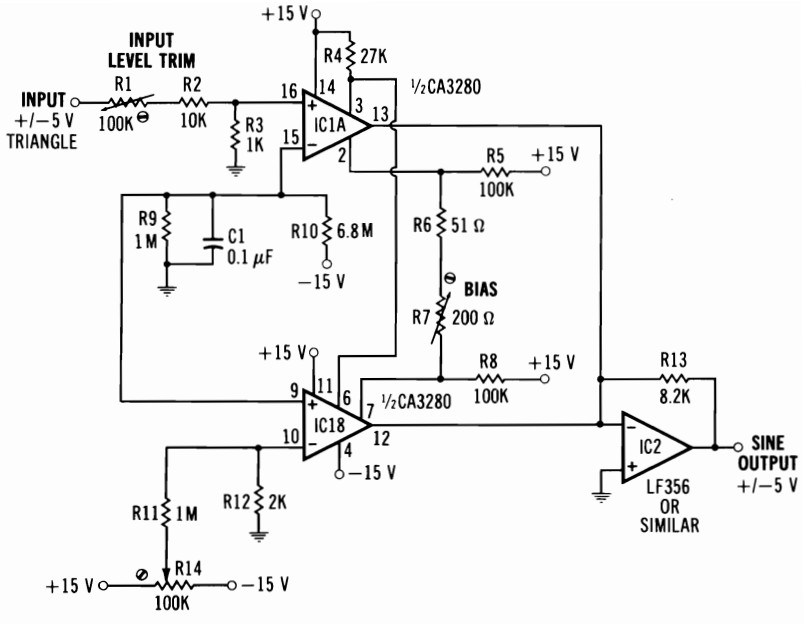



**Fig. 4-11. A triangle-wave to sine-wave conversion circuit using a dual ota.**

adjusted by trimmer R1. The symmetry of the output is adjusted by trimmer resistor R14. Trimmer resistor R7 may be replaced with a 120-ohm resistor. It adjusts the differential amplifier emitter currents between the two ota's.

A discrete circuit for a triangle to sine-wave converter is shown in Fig. 4–12.[8] Its operation is basically the same as the CA3080 circuit just discussed.

Fig. 4–13 is a multifunction waveform converter circuit using an SG1858/CA3054 transistor array to convert a triangle wave to a sine wave and/or to a width modulated pulse waveform.[9] The sine-wave conversion circuitry is the same as in Fig. 4–12. The second half of the IC is used as a comparator to create a width modulated pulse from a sawtooth or triangle-wave input signal.

## CUSTOM VCO CIRCUITS

When function generator ICs, such as the Intersil 8038, were introduced in the early seventies, hobbyists had high hopes of using them in electronic music vco circuits. These ICs, how-

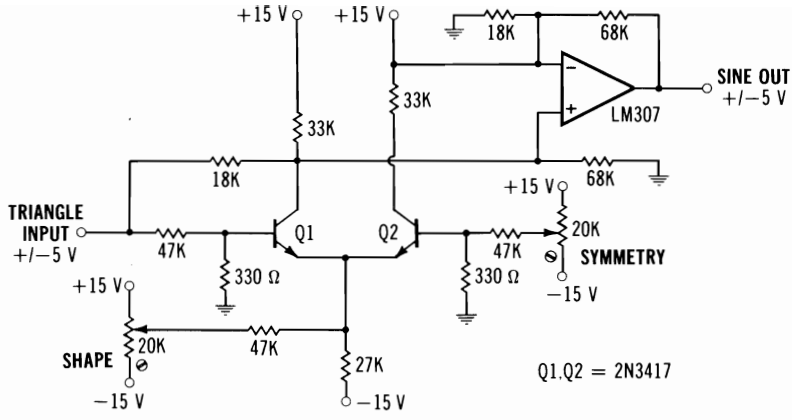



**Fig. 4-12. A triangle-wave to sine-wave converter using discrete transistors.**

ever, generally had too low a frequency range and used linear rather than exponential voltage control. As music synthesizers became more and more popular, a market was created for custom vco ICs that could be used in electronic instruments. Such ICs would reduce cost by cutting down parts inventory requirements, testing time, and pc board space. Solid State Micro Technology for Music was one of the first to introduce such an IC—the SSM2030. This IC performs well enough to be used in polyphonic synthesizers.

A block diagram of the SSM2030 is shown in Fig. 4–14.[10] Exponential converter transistors (commonly called "log" transistors) are provided in the IC. The current controlled oscillator contained in the chip is similar to the circuit (IC2 and IC4) of Fig. 4–9. The exponential current generated by the transistor pair is "mirrored" and used to charge a capacitor. When the voltage across the capacitor reaches the threshold of the comparator, the comparator triggers a one-shot. This one-shot generates a pulse that causes a transistor to turn on and discharge the capacitor. The capacitor voltage is buffered and brought out on pin 6 as a 10-volt sawtooth.

The falling edge of a pulse connected to the "hard sync" input (pin 7) will cause the oscillator to be reset. The same input to "soft sync" input (pin 11) will reset the oscillator only if the internal sawtooth ramp is near (5 percent) the discharge level. This method does not "chop up" the output waveforms as

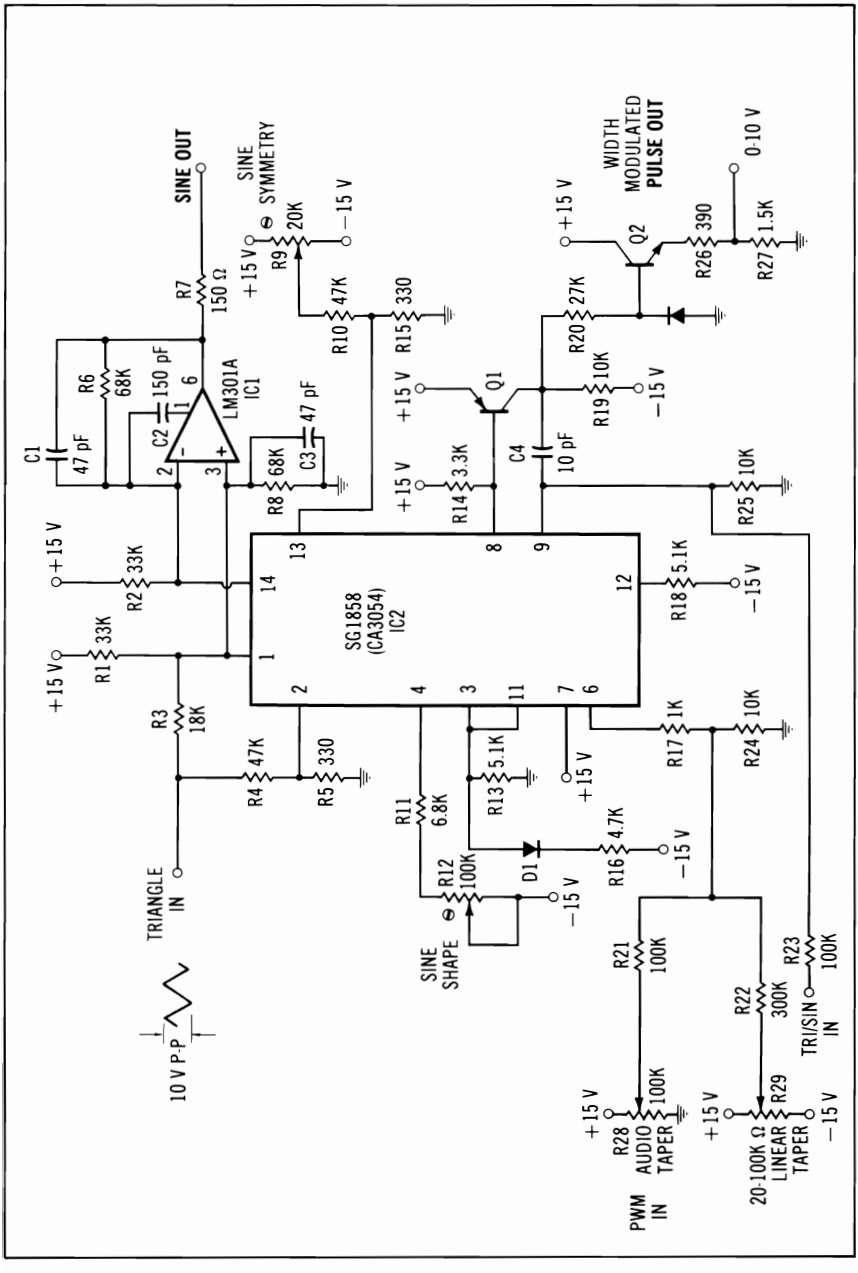



**Fig. 4-13. A multipurpose waveform converter circuit.**

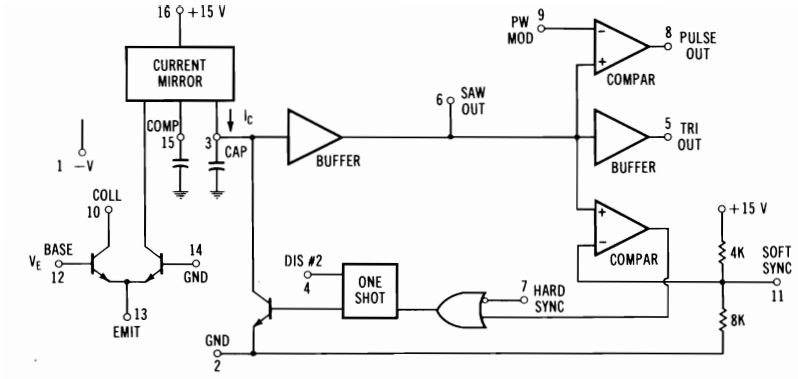



**Fig. 4-14. A block diagram of the SSM2030 vco IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

hard sync does. Typical waveforms for both types of syncing are shown in Fig. 4–15.

An emitter follower in the SSM2030 is biased to generate the top half of the sawtooth waveform at pin 5. The sawtooth is subtracted from this signal by an external op amp to provide a triangle waveform.

An internal comparator in the SSM2030 is available for use in pulse width modulation. Its output appears at pin 8.

Fig. 4–16 shows a complete vco circuit using the SSM2030. The voltage control circuitry should be relatively familiar to you. The elimination of any high-frequency tracking error is accomplished by feeding back a portion of the SSM2030 emitter current at pin 13 through diode D2 and resistor R31 to the base of the first log transistor. Thermal compensation is provided by a positive temperature coefficient (3600 ppm) resistor that is placed in physical contact with the SSM2030. Op amp IC3 and its associated resistors modulate the width of the pulse generated by the 2030. A voltage of 0 to 10 volts on pin 9 of the SSM2030 will vary the pulse width output on pin 5, from 0 to 100 percent. Control R55, IPW (initial pulse width), allows manual control of pulse width with or without a modulation input on the PWM IN control, R53. Op amp IC4 transforms the −0.5- to 7-V pulse output on pin 5 to +/−5 V. Op amp IC5 transforms the 0- to 10-V sawtooth at pin 6 to +/−5 V.

Op amp IC6 subtracts the sawtooth wave from the "half-sawtooth" signal of pin 5 to create a triangle waveform. A low-

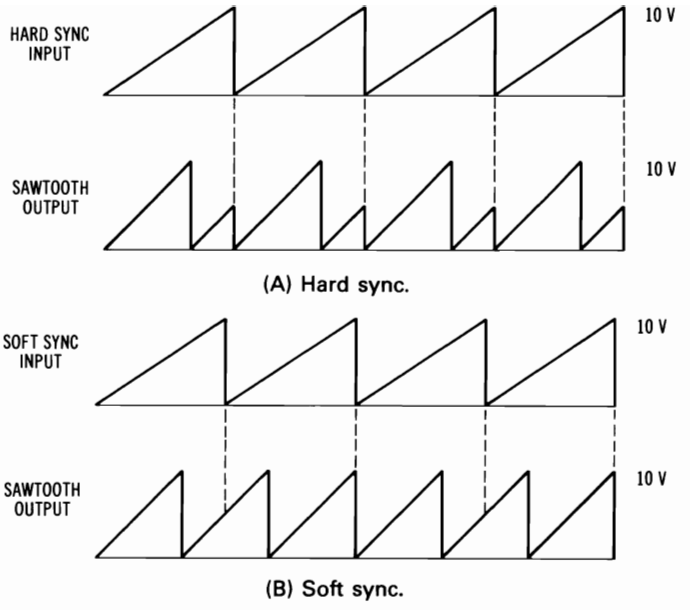
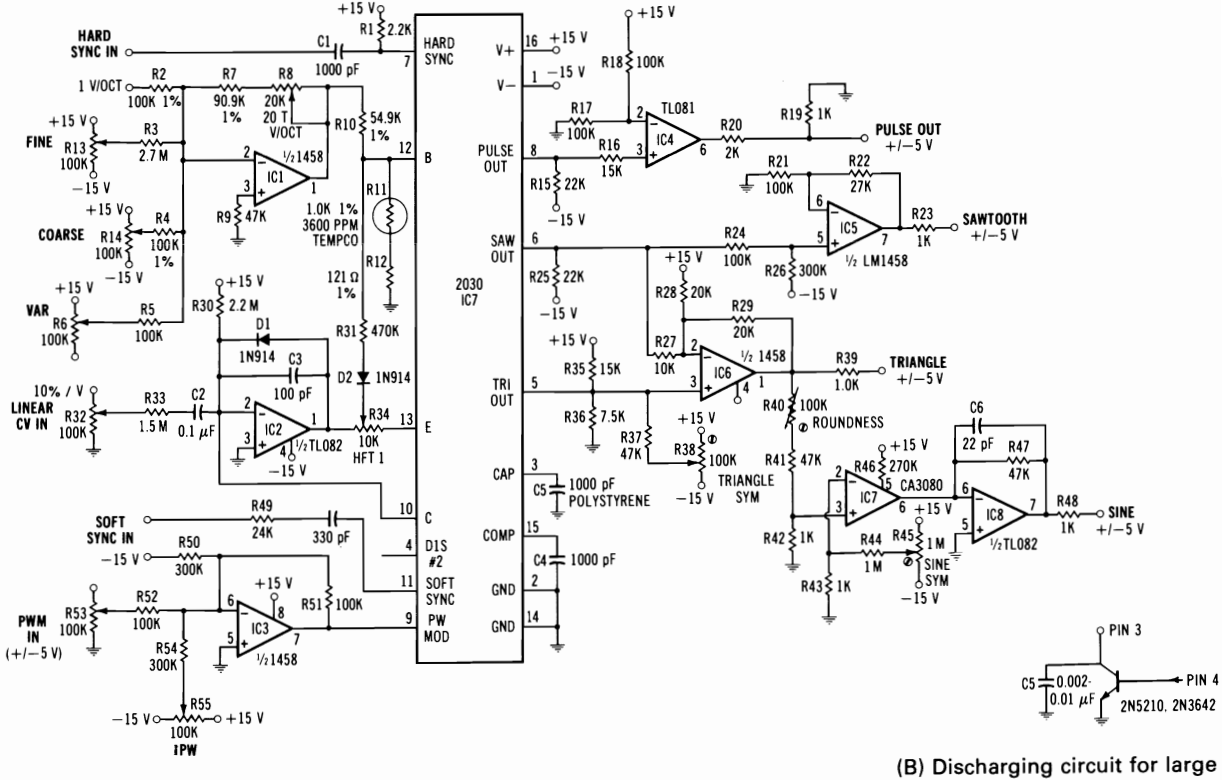



**Fig. 4-15. Examples of hard and soft sync.**

slew-rate op amp, such as a 741, is required here to reduce a switching glitch that occurs at the triangle peaks. Since the slew rate of the op amp is relatively slow, it cannot reproduce the very fast switching glitch. Typical waveforms are shown in Fig. 4–17.

The triangle wave goes into a sine-wave conversion circuit consisting of IC7 and IC8. This circuit closely resembles the circuit used in Fig. 4–7. The total harmonic distortion of the sine wave generated by this circuitry is about 2 percent. Capacitor C5 (pin 3 of the 2030) determines the frequency range of the oscillator. If lower frequencies are desired, this capacitor must be larger. Because of the currents involved, the SSM2030 one-shot should then be used with an external transistor to discharge capacitor C5. Capacitor C5 can have values up to 0.01 $\mu$F. The external discharge circuit ensures a short discharge time and less high-frequency tracking error.

Although the SSM2030 performs well and simplifies vco design, it is not an *ideal* vco chip. The required positive temperature coefficient resistor is not readily available to the hobbyist and is expensive. The requirement of physical contact between




(A) Circuit.

(B) Discharging circuit for large values of C1.

Fig. 4-16. A vco using the SSM2030 IC.

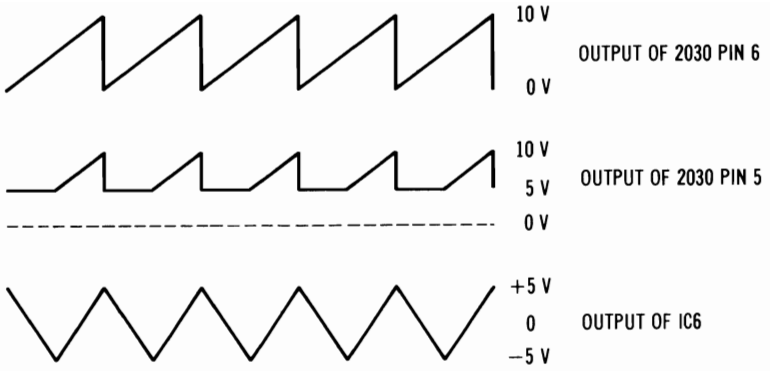



**Fig. 4-17. The signal levels of the sawtooth to triangle-wave conversion circuitry of Fig. 4-16.**

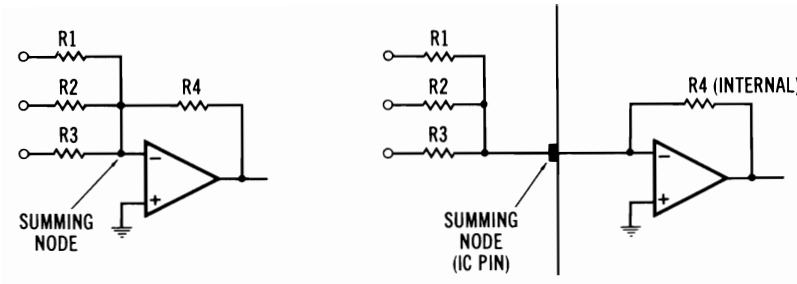
the resistor and the SSM2030 IC makes construction difficult. Also, quite a bit of external circuitry is still required to obtain the control functions and output levels that we desire.

A second generation of vco ICs has since appeared and they simplify designs considerably. The Curtis Electromusic CEM3340/3345 is one such example. *All of the exponential and linear voltage control circuitry is internal to the chip.* The negative input terminals (calling summing nodes) of the internal exponential and linear control voltage op amps (similar to IC1 and IC2 of Fig. 4–16) are brought out to pins on the integrated circuit. Control voltage summing is achieved by simply connecting the various control voltage summing resistors to these points. This is illustrated in Fig. 4–18.

The positive temperature coefficient resistor necessary in the previous vco circuits has been eliminated by a temperature compensation circuit internal to the IC.

Four output waveforms are available from the CEM3340/45. Waveform trimming is unnecessary but external level shifting is required to obtain bipolar (+/−5 V) signals.

Fig. 4–19 contains a complete vco circuit using the CEM3340. The 3340 has an internal 6.5-V zener diode that permits operation from any negative supply from −4.5 volts to −18 volts. For negative voltages greater than −7.5 volts, a series current-limiting resistor is required. This is the function of resistor R14 (pin 3). Its value is determined by the formula: R14 = supply voltage minus 7.2 V/0.008. The positive supply may be




(A) For the LM307. (B) For the CEM3340/3345 IC.

**Fig. 4-18. The summing node.**

from 10 to 18 volts. However, the vco waveform amplitudes are directly related to the positive supply voltage.

Resistors R1 and R2 (wired to pins 7 and 15) set the initial frequency of the oscillator, when no input control voltages are present. With the values shown, the frequency can be adjusted to 65.406 Hz—the frequency of the lowest note on a four-octave keyboard. Resistor R6 functions as a coarse frequency adjustment that varies the output frequency ±5 octaves. Control R7 is a fine frequency adjustment that varies the output frequency ±0.5 octave. Resistor R9 and C1 are required for compensation in the internal op amp. Resistors R11 and R12 adjust the input control voltages so that a precise 1-volt-per-octave output response is produced. Resistor R20 (pin 13) sets the reference current for the exponential converter circuit. Linear frequency modulation is accomplished through resistor R21 and capacitor C4. This input is ac coupled (C4) to prevent an output frequency error due to possible dc drift in the linear control signal. Gain compensation for the internal op amp is provided by resistor R23 and capacitor C5. Capacitor C6 determines the frequency range of the oscillator. If a 0.001-$\mu$F capacitor is used as C6, the vco range is from 5 Hz to 10 kHz.

Temperature compensation for the exponential (current) converter circuit is achieved by multiplying the current sourced into the control pin (pin 15) by a coefficient directly proportional to the absolute temperature. Since the temperature is sensed by transistors that are on the same die as the log transistors, thermal tracking is excellent. Compensation for any high-frequency tracking error caused by the bulk emitter resistance of

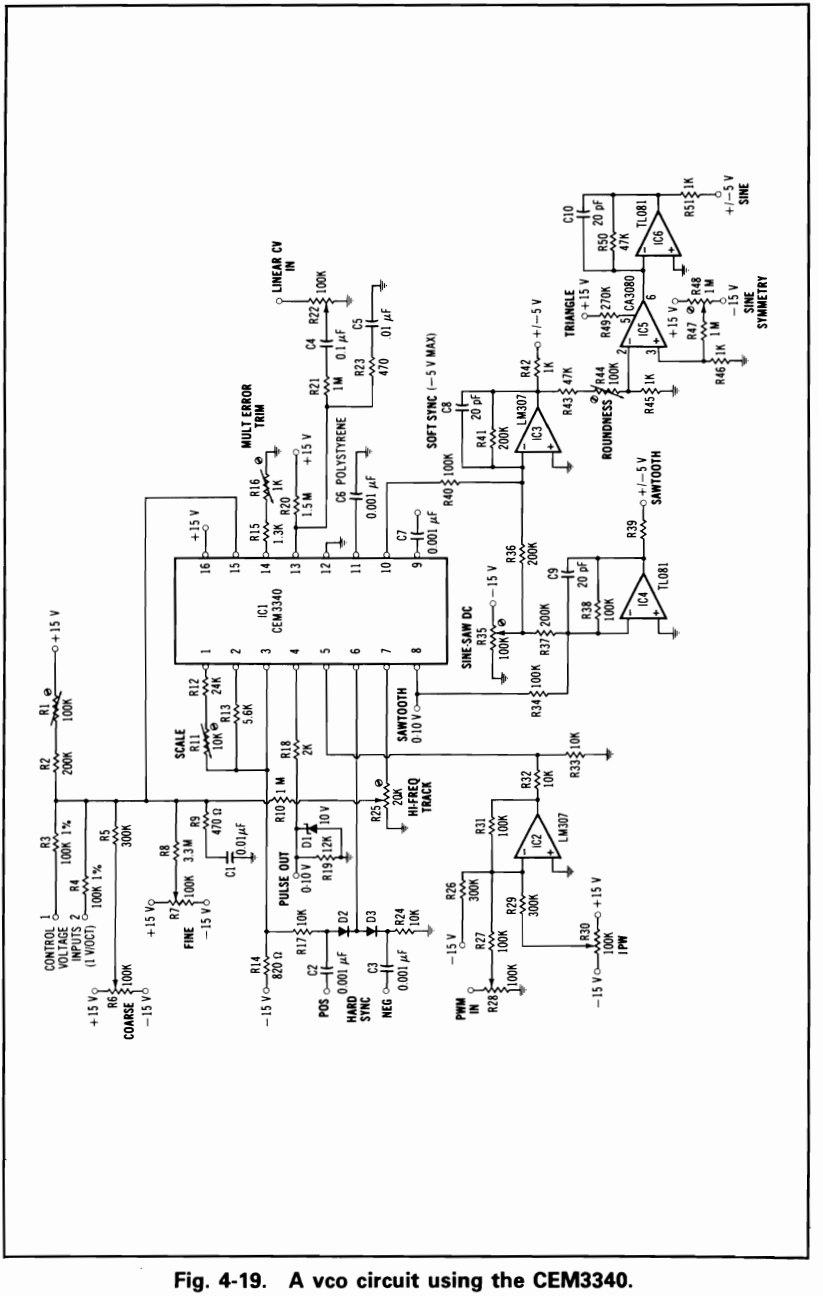



**Fig. 4-19. A vco circuit using the CEM3340.**

the log transistors is achieved by converting the exponential current on pin 7 into a voltage and feeding it back into the control input pin (pin 15). Trimmer R25 is set to minimize high-frequency tracking error. Initially the wiper of R25 is moved to the ground position and the 1 V/OCT scale is adjusted for low octaves with trimmer R11. Trimmer resistor R25 is then adjusted for minimum tracking error between low and high octaves.

The CEM3340 is capable of both hard and soft sync. Soft sync is achieved by applying negative pulses (0 to −5 V) through capacitor C7 to pin 9. *Positive voltages should not be applied to this pin.* If this input is not used, it is recommended that it be bypassed to ground with a 0.1-$\mu$F capacitor to prevent possible triggering due to spikes on the power supplies.

Two variations of hard sync are provided in the circuit of Fig. 4–19. The basic current controlled oscillator in the CEM3340/45 generates a triangle wave. Hard sync causes the triangle ramp to reverse direction. A positive pulse applied to the positive sync input in Fig. 4–19 will force a rising triangle waveform to reverse direction. A negative pulse applied to the negative sync input causes a falling waveform to reverse direction. The pulse signals into the sync pin (pin 6) should be from 0 V to a maximum of 3 V.

Pulse width modulation is achieved by a 0- to 5-V level on pin 5 of the CEM3340. Op amp IC2 and its associated resistors R26–R33 allow manual and/or external control over the pulse width. The pulse output of 3340 appears on pin 4. The level at this pin is normally 0 to 12 volts for a 15-V positive supply. A zener diode (D1) is used to drop this level to 0 to 10 V. This can be level shifted to +/−5 V, if desired. The pulse output on pin 4 will have a slower fall time compared to the rise time, due to limitations in the internal comparator. An external circuit such as Fig. 4–20 can be used for faster rise/fall times.

Op amps IC3 and IC4 in Fig. 4–19 condition the sawtooth and triangle outputs of the CEM3340 to +/−5 V. *Load variations on the triangle output of the CEM3340 (pin 10) vary the frequency of the oscillator.* Therefore a buffer or constant load is required for this pin if it is used. Triangle to sine-wave conversion is achieved by the circuitry of IC5 and IC6.

Not to be outdone, Solid State Micro Technology for Music has recently introduced the SSM2033 vco IC. This is an im-

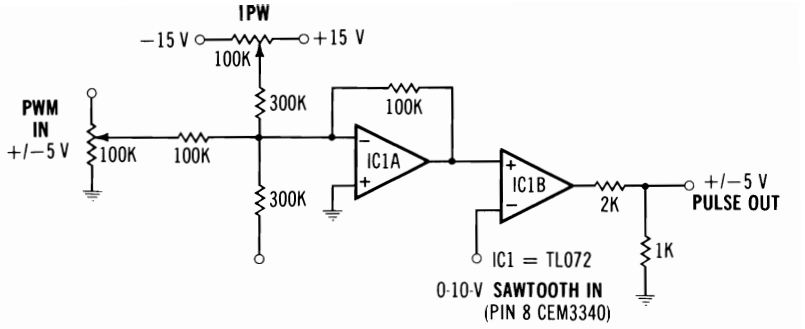
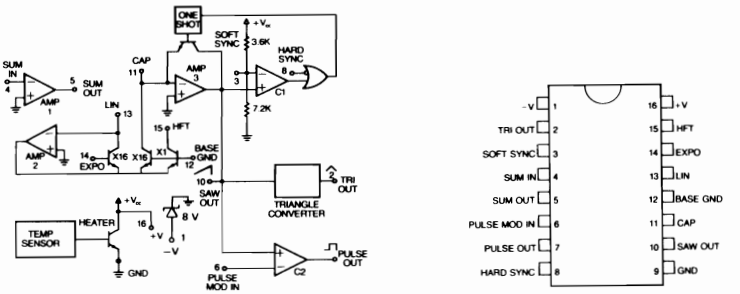



**Fig. 4-20. A pulse-width modulation circuit.**

proved version of the SSM2030, with much more of the required control and waveform conversion circuitry built into the IC. The positive temperature coefficient resistor is eliminated by an internal circuit that regulates the temperature of the IC to a level (55°C) above the ambient temperature. The IC will draw a relatively high supply current (10–37 mA) due to the requirements of the internal heater. This current will decrease as the ambient temperature rises.

A block diagram of the SSM2033 is shown in Fig. 4–21A.[11] The circuitry resembles that of the SSM2030 in that the basic current controlled oscillator generates a sawtooth waveform. The two log transistors in the exponential converter *each contain 16 paralleled transistors.*. This reduces the bulk emitter resistance and high-frequency tracking errors. A third transistor




(A) Block diagram. (B) Pinout (top view).

**Fig. 4-21. A block diagram and IC pinout of the SSM2033 vco.** *(Courtesy Solid State Micro Technology for Music, Inc.)*

generates an exponential current to enable further trimming of the high-frequency tracking error. A diagram of the voltage control circuitry is shown in Fig. 4–22.[12]

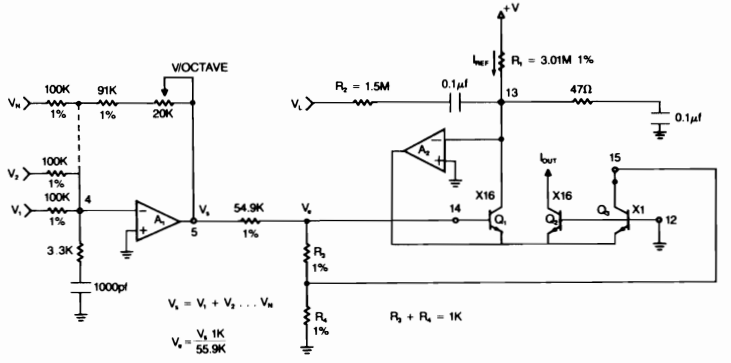



**Fig. 4-22. A diagram of the voltage control circuitry of the SSM2033.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

The SSM2033 will operate with positive supplies from 9 to 18 V with the output waveforms being level dependent. The negative supply can range from −4.5 to −18 V with a series current-limiting resistor required for negative voltages greater than −6 V.

Fig. 4–23 contains a vco circuit using the SSM2033. The external circuitry closely resembles that of Fig. 4–19. Capacitor C6 determines the frequency range of the oscillator. Increasing its value will lower the frequency range of the circuit.

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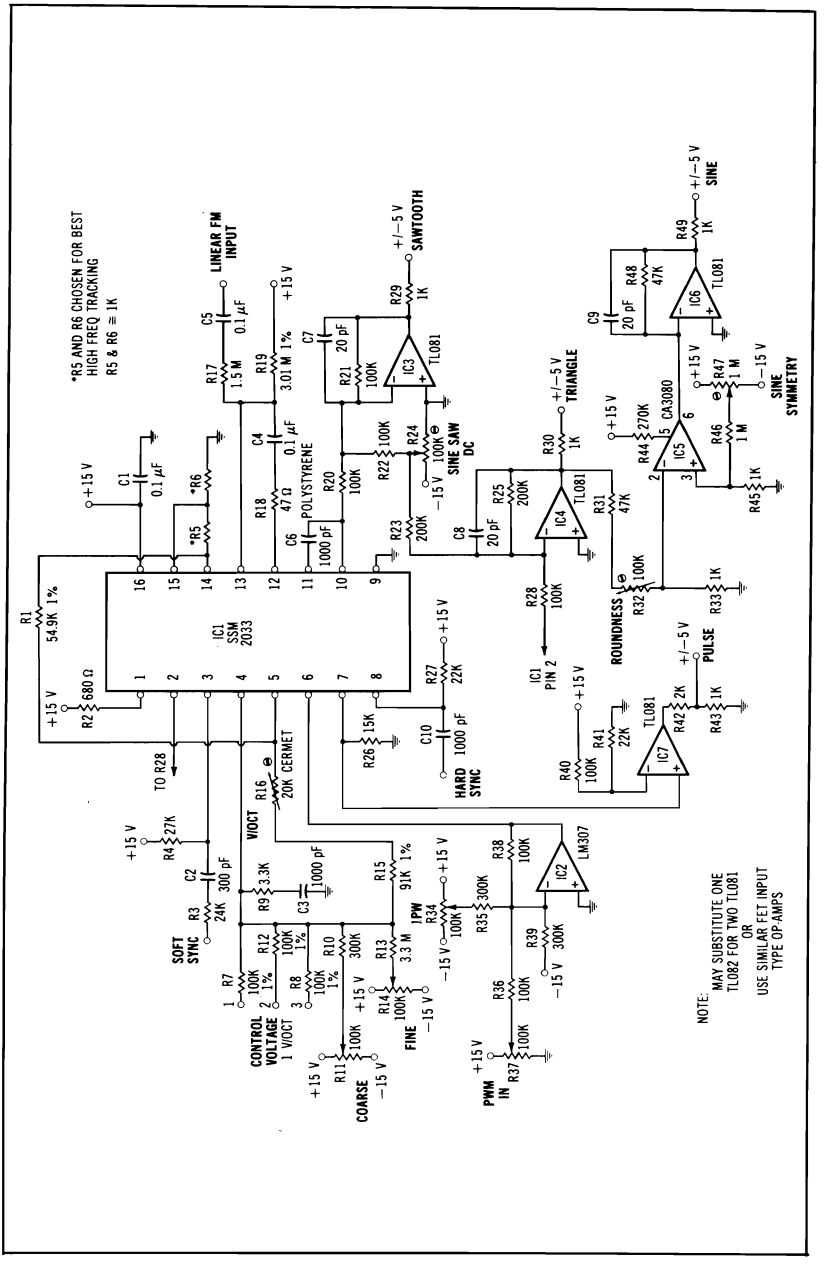
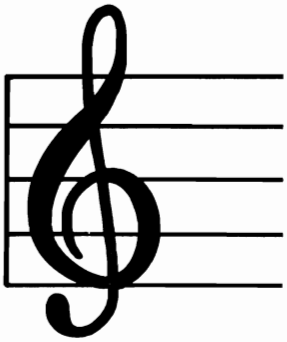



**Fig. 4-23. A vco circuit using the SSM2033 vco IC.**

7. See No. 4 above.
8. *CFR Technotes,* No. 11.
9. *CFR Technotes,* Vol. 3, No. 5, pp. 4—5.
10. Solid State Micro Technology for Music, Santa Clara, CA.
11. Solid State Micro Technology for Music, Santa Clara, CA.
12. Solid State Micro Technology for Music, Santa Clara, CA.

# CHAPTER 5

# FILTERS



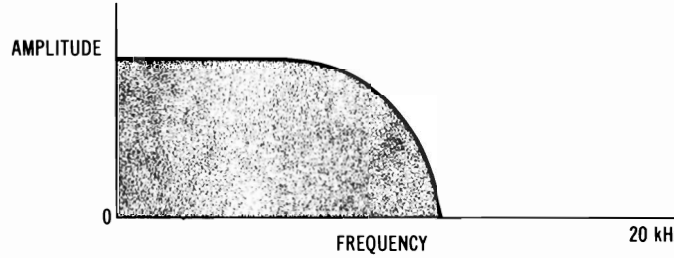
A filter is generally used to attenuate or reduce the amplitude of certain frequency portions (timbre) of an input signal to change its sound or "tonal character." As discussed in Chapter 1, the waveforms generated by a vco (sawtooth, triangle, etc.) will consist of a fundamental frequency and, except for the sine wave, several frequencies, called harmonics, that are multiples of the fundamental (see Figs. 1–2 and 1–3). These waveforms sound different from each other but have a constant frequency and become dull to listen to in a short time. Their function is to provide a broad range of frequencies for the filter(s) to alter. This is the fundamental concept of subtractive synthesis, which was explained in Chapter 1. A *voltage controlled filter*, or *vcf*, can be used to dynamically change the frequency content of a vco waveform. The magnitude of the control voltage will determine what frequency portion(s) of the input signal the vcf will affect.

## FILTER BASICS

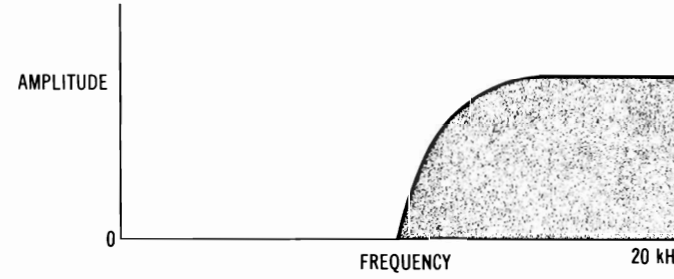
Filters are characterized by the frequency portion of the input signal they allow to pass through, unattenuated, to the output. Some of the more typical filter *responses* are illustrated in Fig. 5–1. The most popular type of filter used in electronic music, the *low-pass* filter (lpf), passes low frequencies and attenuates higher frequencies. A *high-pass* filter (hpf) does just the oppo-

site. A *bandpass* filter (bpf) attenuates those frequencies higher and lower than the desired pass frequency. An *all-pass* filter shifts the *phase* of an input signal. As a very simple example, the all-pass filter would delay the signal as it passes through the filter. Thus, if we look at both the input and output signals, the minimum and maximum of the output signal will not occur at the same time as those of the input signal. Thus they are out of phase. Higher frequencies are shifted more than lower frequencies with this type of filter. When the shifted signal is summed with the input signal, notches are created in the frequency response where the two signals are 180° out of phase (a half-cycle apart). This type of filter produces the popular "phase shifter" sound often used with an electric guitar.

The rate of a filter's attenuation is called its *rolloff*. The sharper the rolloff is, the more noticeable the filter's effect becomes. Filter rolloffs are specified in terms of *decibels per octave*. The decibel (dB) is a unit of measure for comparing




(A) Low-pass response.




(B) High-pass response.

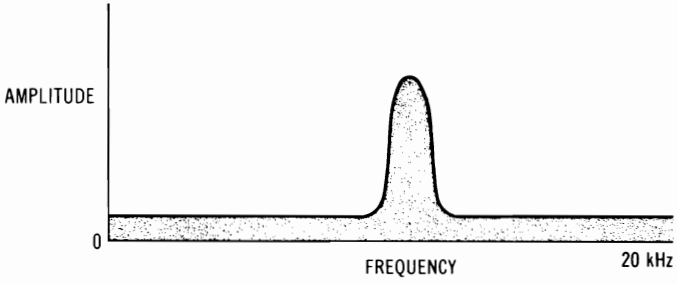
**Fig. 5-1. Command**

relative signal levels in a circuit. The formula for measuring decibels for voltages $V_1$ and $V_2$ having equal impedances is

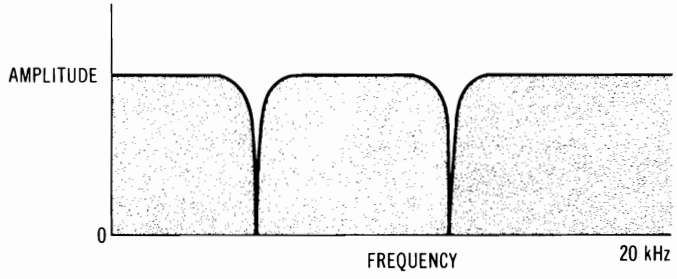
$$dB = 20 \log (V_2/V_1)$$

A chart of common decibel ratios is given in Fig. 5–2. Typical rolloffs of filters used for electronic music range from −3 dB/octave to −24 dB/octave.

The point in a filter's frequency response at which the rolloff approaches −3 dB/octave (0.7079) is called the filter's *cutoff frequency.* If you have a sine wave generator (or vco), an oscilloscope, and a frequency counter, you can determine the cutoff frequency of a filter by using the method shown in Fig. 5–3. The sine wave generator is first adjusted to a frequency in the filter's passband. The signal level of the generator or the vertical gain of the oscilloscope is adjusted for a 4-cm peak-to-peak (±2 cm) display on the oscilloscope screen. Then the sine wave




(C) Bandpass response.




(D) All-pass "phase shifter" response.

**filter responses.**

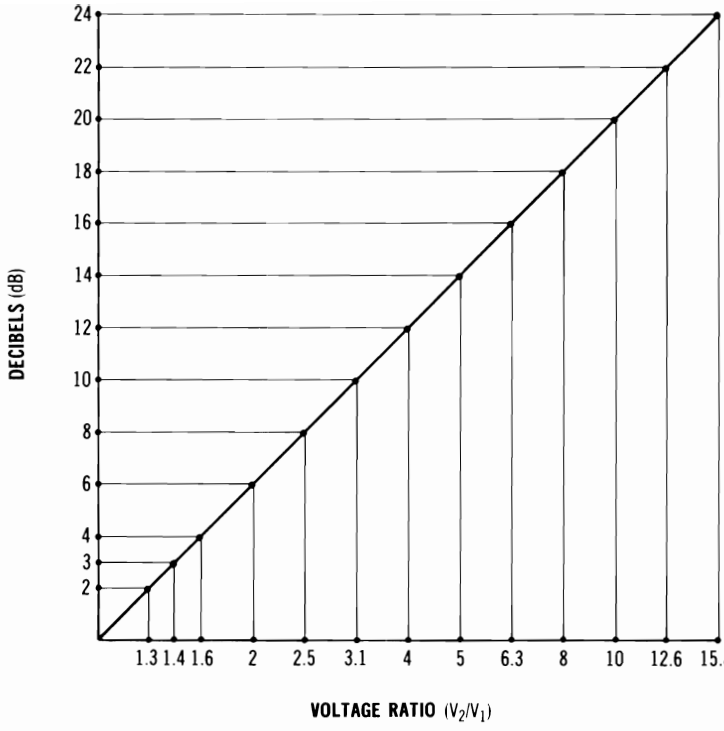



**Fig. 5-2. Decibel conversion chart.**

generator frequency is adjusted until the output level of the filter drops to 2.8 cm peak to peak (± 1.4 cm). The frequency at this point will be the cutoff frequency of the filter.

The method detailed in Fig. 5–4 can be used to observe the frequency response of a filter. If your oscilloscope does not have an external horizontal (Y) input, you will probably experience some difficulty in syncing your scope to observe the full frequency sweep.

Often, *resonance* is added to a filter (by feeding back the filter's output) to create a peaking of the amplitude at frequencies near to and including the cutoff frequency of the filter. If the resonance (or *Q*) is increased, the filter will begin to oscillate at a frequency at or near the cutoff frequency. Because this oscillation is often a pure sine wave, many sine wave generators use this method to generate their output signal. The effect of

resonance in a low-pass filter is shown in Fig. 5–5. Increasing the resonance in a bandpass filter will sharpen the rolloff and peak the response amplitude at the filter's designed center frequency. The circuit's $Q$ is defined as the filter's center frequency divided by the filter's bandwidth (defined as the difference in frequency between the two cutoff frequencies). Higher $Q$'s mean sharper frequency responses. This concept is illustrated in Fig. 5–6.

*Resonant filter banks* (sometimes called responding filter banks) are designed with a group of high-$Q$ bandpass filters that are all fed the same input signal. The filter outputs are summed in a proportion determined by the user to obtain a desired output timbre. A common filter bank is the *graphic equalizer,* used in pa systems and recording studios. Fig. 5–7 shows a filter bank using bandpass filters.

If the resonance of a filter is set so high that the filter is close to the point of oscillation, a sharp pulse fed into such a filter will cause it to ring or oscillate for a short time at the filter's center frequency (Fig. 5–8). This effect is utilized in many rhythm percussion boxes to simulate congas, drums, and so on.

The complexity of a filter circuit is directly related to its rolloff rate. A simple *passive* filter, using only a resistor and a capacitor, has a rolloff of −6 dB/octave (see Fig. 5–9A). This matches the curve of the capacitive reactance for the circuit. The *order* of a filter relates to the number of such *RC* sections in a filter circuit. The simple *RC* filter is a first-order filter. A simple *active* low-pass filter, using an op amp, two resistors, and two capacitors (such as the one shown in Fig. 5–9B), is a second-order filter.

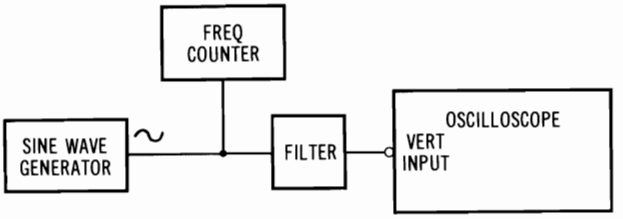
The order of a filter circuit also relates to the number of frequency *poles* it contains. A frequency pole is the cutoff frequency of an *RC* circuit in the filter circuit. A fourth-order low-pass filter may have four poles of the same frequency or of scattered frequencies. A sharper rolloff is obtained if the poles are slightly scattered. However, the audible difference is not worth the extra design effort if the filter is to be voltage controlled. The majority of filter circuits used in electronic music are made up of combinations of second-order filters. Generally, a fourth-order filter can be made by cascading two second-order or four first-order filters. The sharpness of a filter's rolloff is directly related to the filter's order by

rolloff slope = filter order × −6 dB/octave

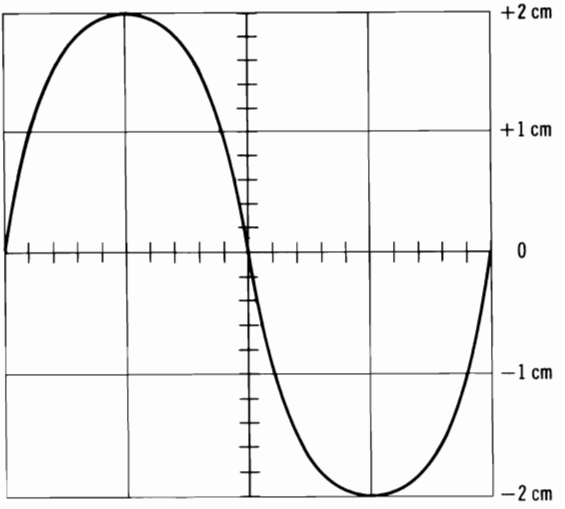
which is illustrated in Fig. 5–9C.

## VOLTAGE CONTROLLED FILTERS

The voltage controlled filter (vcf) is one of the most valuable modules in a synthesizer. Much of the difference in sound you may notice between different synthesizers is due to the design of each unit's vcf. All manufacturers place a lot of effort into the




(A) Equipment setup.




(B) Passband frequency adjusted to +/−2 cm.

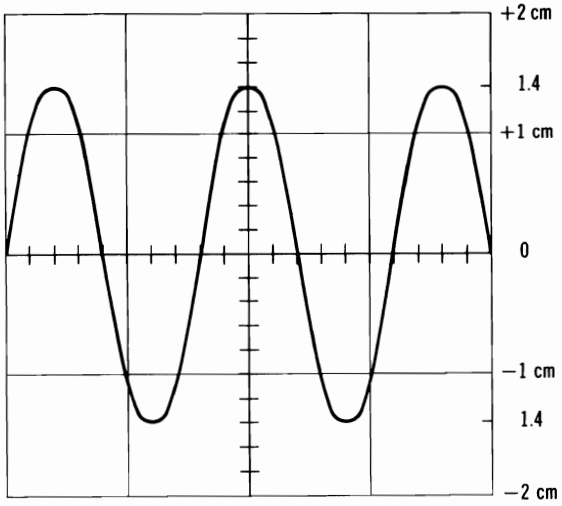
**Fig. 5-3. A method for finding**

design of their vcf circuit(s) since they realize that the result will affect the synthesizer's sound capabilities. Generally, a higher-order vcf is more useful than a lower-order vcf. The closer a filter's rolloff approaches a complete cutoff, the more impressive it sounds. As mentioned earlier, to obtain higher-order filters lower-order filters are cascaded (put in series). Each stage in the filter is identical in design.

A typical first-order low-pass filter is shown in Fig. 5–10. At low frequencies the capacitor is effectively out of the circuit and the circuit is an inverter with a gain that is determined by the resistors (usually unity gain). At higher frequencies, however, the capacitor begins to look more and more like a resistor and finally assumes a resistance less than the effective resistance of resistor $R_f$. Thus the output will have a frequency-dependent gain, $A$, found by the formula

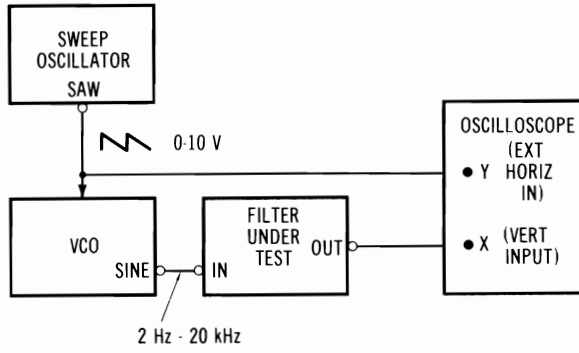
$$\frac{X_C \times R_f}{X_C + R_f} \times \frac{1}{R_i} = A$$

which, at very high frequencies, approaches $X_c/R_i$ or $1/2\pi f R_i C$, where $X_C$ (capacitive reactance) = $1/2\pi f C_f$. Since the gain de-

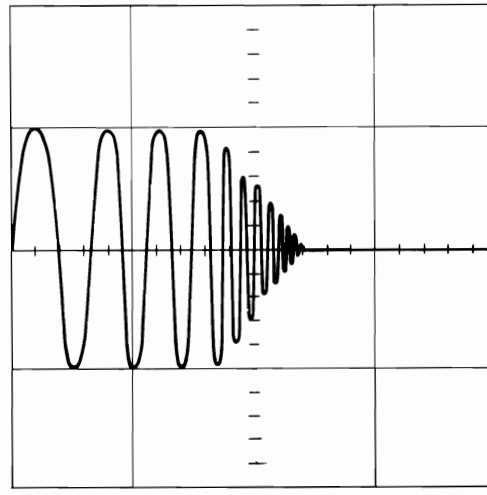



(C) Sine frequency adjusted for +/−1.4 cm = cutoff frequency of filter.

**the cutoff frequency of a filter.**



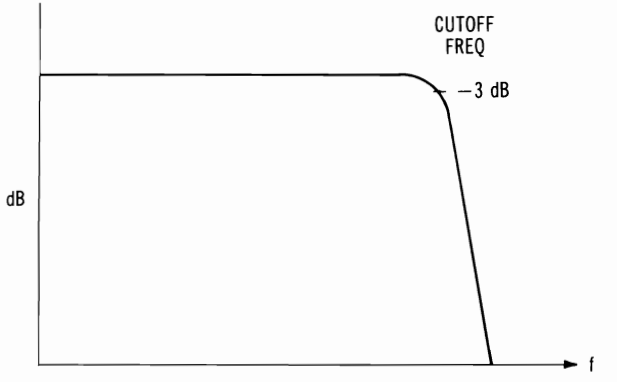

(A) Test method.



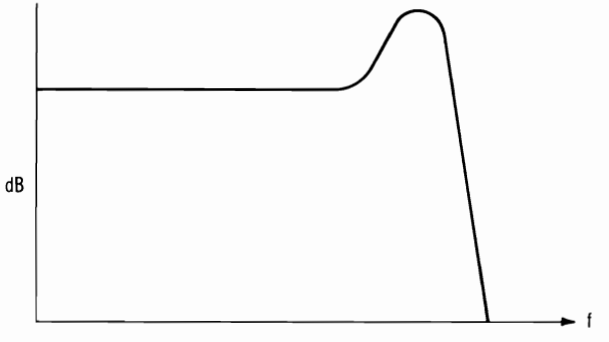
(B) Sample low-pass response.

**Fig. 5-4. A method for observing the frequency response of a filter.**

creases at a rate of $1/f$, we see that for a 1-octave change the gain is ½, for a rolloff of −6 dB. What remains is to find a way to control the cutoff frequency of the filter circuit by applying a voltage to it. This is where the ota comes to the rescue. Several voltage-controlled, first-order, low-pass filters using ota's are shown in Fig. 5–11. The signal is attenuated before being fed into the ota to prevent overdriving the input (we don't want a triangle-wave to sine-wave converter here!). The input signal




(A) Low-pass response, no resonance.




(B) Low-pass response, resonance added.

**Fig. 5-5. Adding resonance to a low-pass filter.**

will cause the ota output to generate a proportional current with a gain set by the control current ($I_C$). This output current is used to charge a capacitor. The charging rate of the capacitor will increase as the control current increases. If the input signal to the ota is faster (high frequency) than the charging rate of the capacitor, the average voltage level (of the signal with respect to time) across the capacitor will be less than the level of the input signal. This is the basic low-pass function. Some feedback is required (by means of the resistor in the feedback loop) to prevent the capacitor from becoming completely charged, due to dc offsets that may occur in the ota.

Fig. 5–11A shows an lpf section that uses a FET buffer which was common a few years ago. Distortion tends to increase with

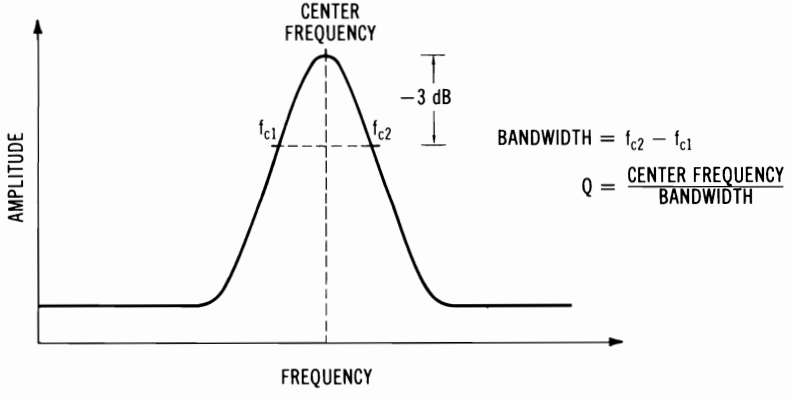



**Fig. 5-6. Determining the bandwidth and *Q* of a bandpass filter.**

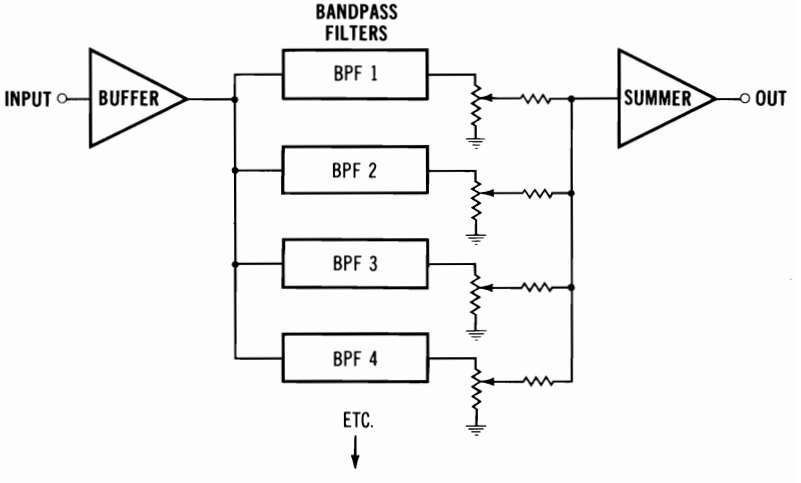



**Fig. 5-7. A filter bank.**

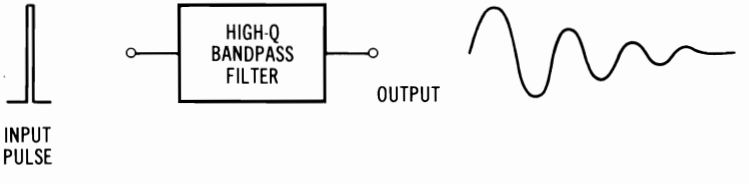
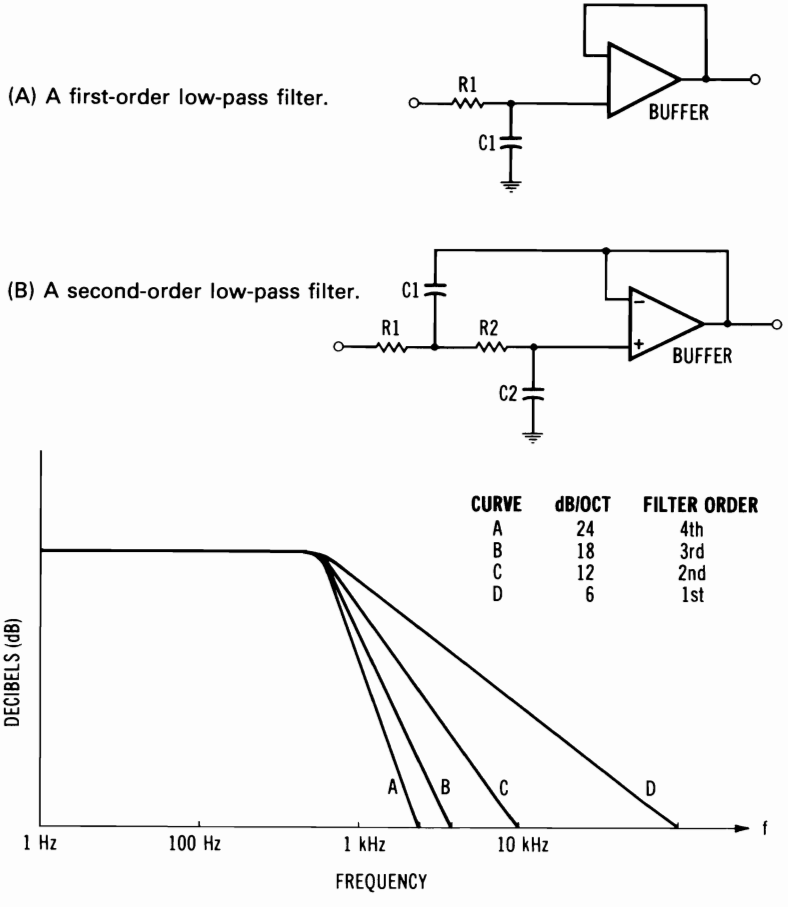



**Fig. 5-8. Making a bandpass filter "ring."**




(C) Frequency response with different rolloffs.

**Fig. 5-9. Low-pass filter sections and common response rolloffs.**

signal level when using a FET in such a circuit. In Fig. 5–11B the FET is replaced with a FET-input op amp. The input impedance of the op amp must be very high to prevent loading of the storage capacitor. In Fig. 5–11C the capacitor is placed in the feedback loop of the FET op amp, forming a traditional integrator. Note that the input signal is fed into the inverting input of the ota. This is to avoid phase inversion at the output caused by the op-amp integrator. In Fig. 5–11D an lpf section is

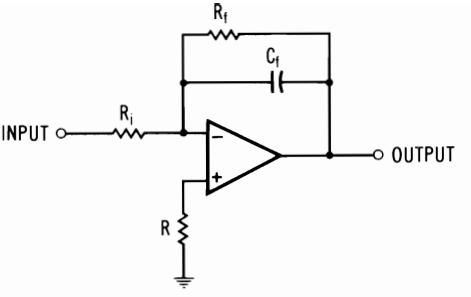


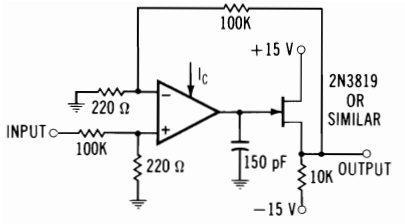

**Fig. 5-10. A first-order low-pass filter.**

constructed using the internal buffer in the LM13600/NE5517. This buffer may cause problems in some circuits due to its typical −1.4-V offset. It can be left out and the circuit can be configured as in Fig. 5–11C, if desired. By adding and/or moving a few components of the basic lpf section in Fig. 5–11B, other filters can be constructed, as shown in Fig. 5–12.

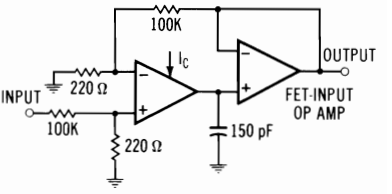
An exponential current source (for $I_C$) is required to control the filter sections to achieve the wide control range we desire and to enable the filter to track at 1 V/octave. Custom ICs are now available that contain four user-adaptable gain cell/buffer stages that are controlled by a common current ($I_C$) from an internal exponential current source. Since these are all in one IC, interstage tracking is excellent. The design of several filter structures is simplified due to the "building block" structure of the ICs. Some of these ICs will be discussed in the next section of this chapter.

### Voltage Controlled Low-Pass Filter Circuits

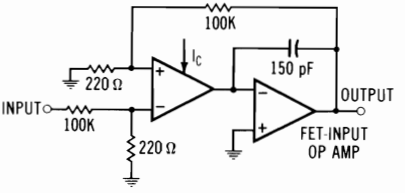
The most popular filter used in electronic music is the voltage controlled low-pass filter. A block diagram of a four-pole low-pass filter is shown in Fig. 5–13. Four cascaded single-pole filters are driven by an exponential current. At low frequencies the output will be in phase with the input, because these frequencies are in the passband of the filter. High frequencies (above cutoff) will be shifted 360° and thus will also be in phase with the input. However, frequencies near the cutoff frequency will be shifted almost 90°. If the filter's output is inverted (as shown in Fig. 5–13) and fed back, the amplitudes of frequencies at and around cutoff will be increased (resonance). If this



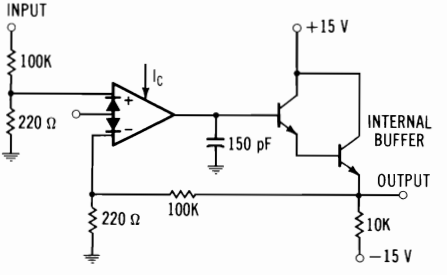

(A) Using an FET buffer.




(B) Using a op amp as a buffer.




(C) Using a op amp as a integrator.

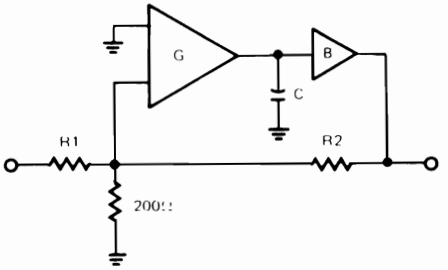



(D) An LM13600/NE5517 circuit using an internal buffer.

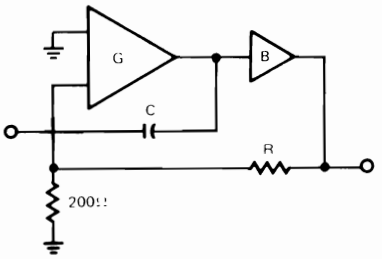
**Fig. 5-11. Several voltage (current) controlled low-pass filter sections.**

feedback is increased, the filter will oscillate at or near the cutoff frequency. The design and construction of such a filter can be achieved with discrete ota's (CA3080, CA3280, etc.) and an exponential current converter similar to those used in the last chapter. However, it is easier and better to use one of the custom ICs available.

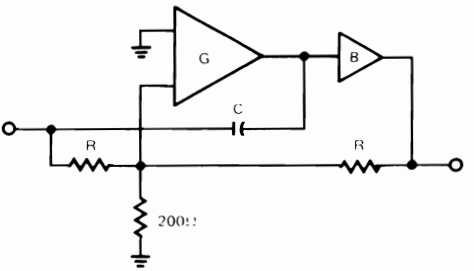
A discrete circuit probably will not track as well, will have




(A) Low-pass real pole.




(B) High-pass real pole.




(C) All-pass phase shift.

**Fig. 5-12. Basic filter section design using transconductance amplifiers.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

control voltage offsets that will have to be trimmed out, and will end up costing almost as much as a custom IC. Custom ICs have an excellent signal-to-noise ratio (typically 90 dB), low distortion (0.02 percent), and high *control-voltage rejection* (low control voltage feedthrough to the filter circuit, signified by "popping" or changes in the average dc level of the signal).

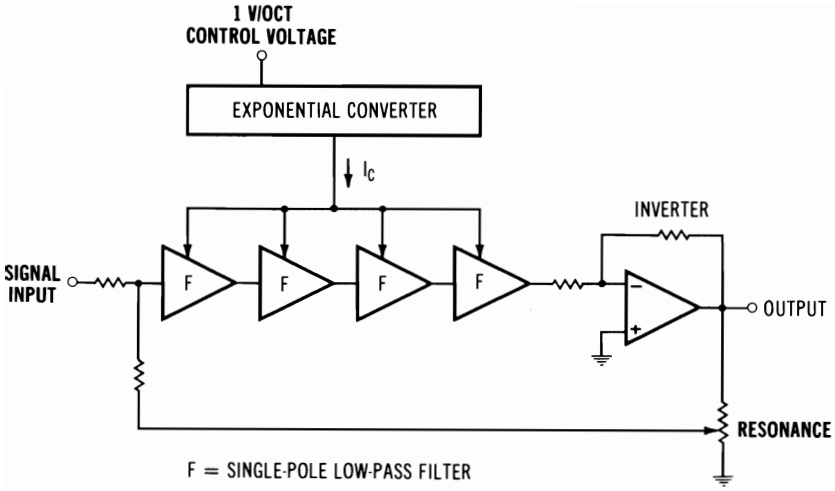
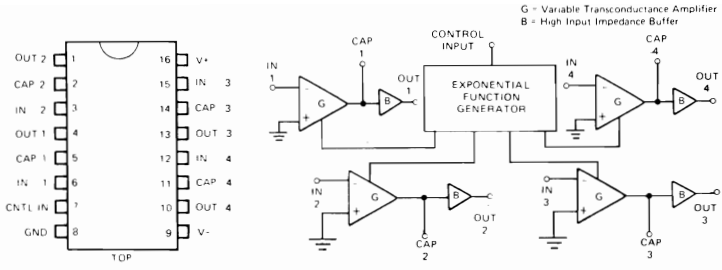



**Fig. 5-13. Block diagram of a four-pole, low-pass filter.**

A pin diagram and functional block diagram of the SSM2040 vcf IC appears in Fig. 5–14. This IC contains an exponential current converter and four gain/buffer stages. This IC is used in a four-pole voltage-controlled lpf in Fig. 5–15. A temperature compensating resistor (R8) is wired to pin 7 for temperature stability. The resonance (*Q*) circuitry (IC4–IC6, Q1, Q2) can be replaced with a potentiometer for manual-only control. Op amps IC4 and IC5 form a current controlled amplifier. The current output of ota IC4 is converted to a voltage by IC5. The control voltage from IC6 is converted to an exponential current by transistors Q1 and Q2. These transistors should be close to each other for accurate thermal tracking. The LM13600 may be replaced with another type of ota or a voltage controlled amplifier IC (see next chapter) if desired. If using the LM13600 the control voltage rejection trimmer (R28) must be adjusted for minimum dc shift in the output signal as the "initial *Q*" control (R34) is varied.

The basic filter in this circuit is equivalent to that of Fig. 5–13. The input signal is attenuated by R10 and R12 to have a 20-mV maximum input (peak to peak) at 0.02 percent total harmonic distortion and a signal-to-noise ratio of 90 dB. The values of R12, R15, R18, and R21 (200 ohms) were chosen for the best control voltage rejection by the filter. The value of capacitors C1




(A) Pin diagram. (B) Block diagram.

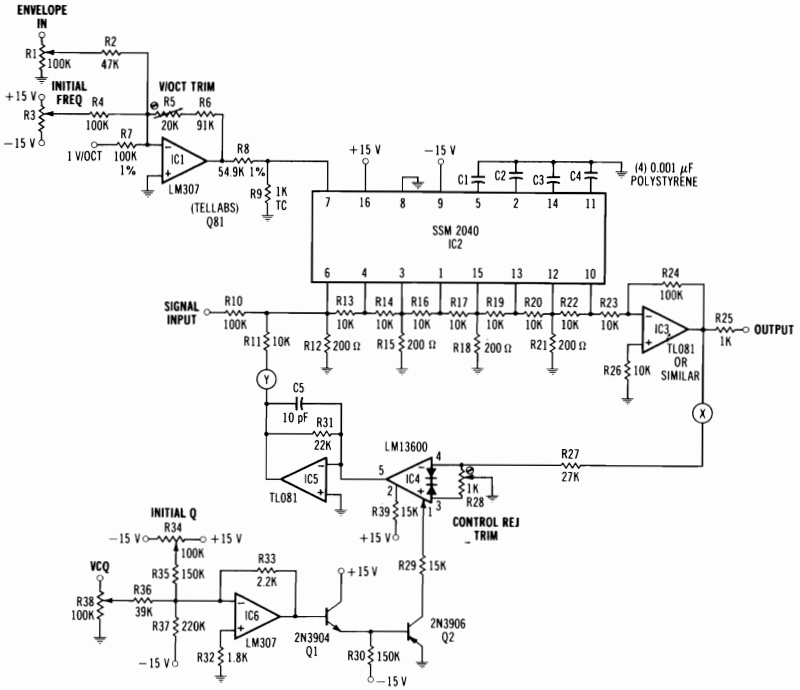
**Fig. 5-14. The SSM2040 vcf IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

to C4 should be at least 1000 pF for stable operation at all control settings. Increasing the value above 1000 pF (0.001 $\mu$F) will lower the range of the filter. Op amp IC3 inverts and amplifies the filter output for unity gain.

Realizing that many SSM2040 ICs were being used for voltage controlled, low-pass filter circuits, such as in Fig. 5–15, SSM decided to introduce an IC optimized for the application, the SSM2044. This IC eliminates the necessity of the external resistor ladder network (10 kilohms, 200 ohms). It also has voltage controlled resonance capability on the chip. Like the SSM2040, the SSM2044 has a high signal-to-noise ratio of 90 dB and very little control voltage feedthrough into the filter.

A block diagram and pin diagram of the SSM2044 is shown in Fig. 5–16. A graph of the filter's performance with $Q$ is shown in Fig. 5–17. At minimum $Q$ it is a gradual rolloff approaching 24 dB per octave at high frequencies. As the $Q$ is increased, the low frequencies are suppressed and frequencies near the cutoff frequency are emphasized. At high-$Q$ settings the filter will oscillate with a sine wave at the cutoff frequency. As can be seen from the second graph, $Q$ increases slowly at first and then rapidly increases with larger amounts of feedback.

A voltage controlled, low-pass filter using the SSM2044 is shown in Fig. 5–18. A reverse audio potentiometer (R9) is recommended for the $Q$ control to give a linearlike control over $Q$. Resistor R10 in the $Q$ control circuit "biases up" the control pin (pin 2) to operate in the most effective voltage range. Oscillation will occur at 7.5 V with the value shown for R7 (15 kilohms). Capacitors C1 and C2 (pins 1 and 15) provide stable resonance




(A) Circuit.

(B) Manual-only *Q* control.

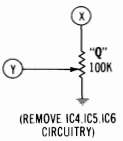
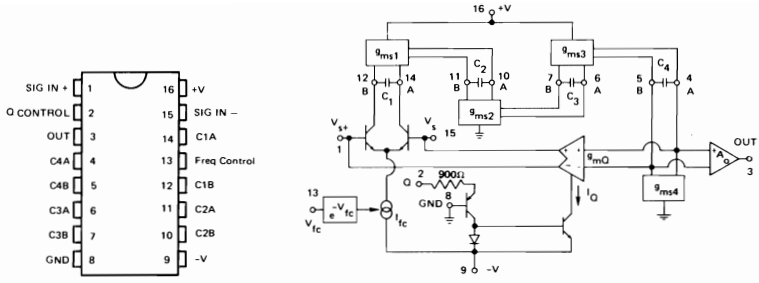


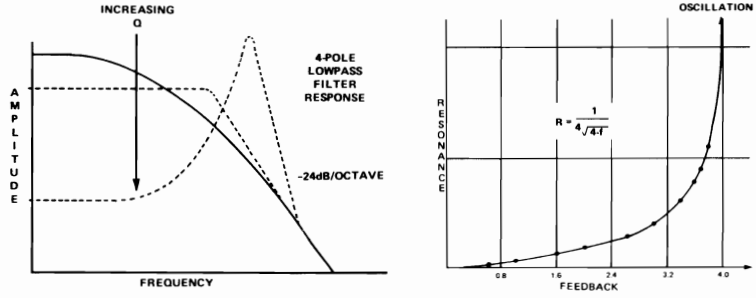

**Fig. 5-15. A four-pole, voltage controlled, low-pass filter using the SSM2040.**

over the sweep frequency range of the filter. Two differential inputs are provided for input signals up to ± 18 V peak to peak. Input resistors R1 and R6 scaled to create a 3-dB-level difference between inputs. This is for use in polyphonic systems where each filter will be used with a voice containing two oscillators. A level difference is necessary to prevent signal cancellation that would occur as one oscillator comes in phase with the other. Op amp IC1A converts the current output of the




(A) Pin diagram. (B) Functional block diagram.

**Fig. 5-16. The SSM2044 vcf IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*




(A) Amplitude vs. frequency. (B) Resonance vs. feedback.

**Fig. 5-17. The effect of increasing resonance on the SSM2044 filter response.** *(Courtesy Solid State Micro Technology for Music, Inc.)*

SSM2044 to a voltage. Resistor R14 (pin 13) should be a Tel Labs Q81C positive temperature coefficient resistor if the filter is to be used as a tracking oscillator (high-*Q* setting). If precision is not required, this resistor can be 1 kilohm, 1 percent, and resistors R15 and R16 can be replaced with 300 kilohms at 1 percent.

The *Q* rejection and frequency offset trimmers shown are optional. The *Q* rejection trim (R4) minimizes *Q* control feedthrough. The frequency offset trimmer (R20) is used to match several identical filters in a polyphonic system for the same frequency sweep range with identical control voltage inputs.

The control voltage input attenuator (R13 and R14) is de-

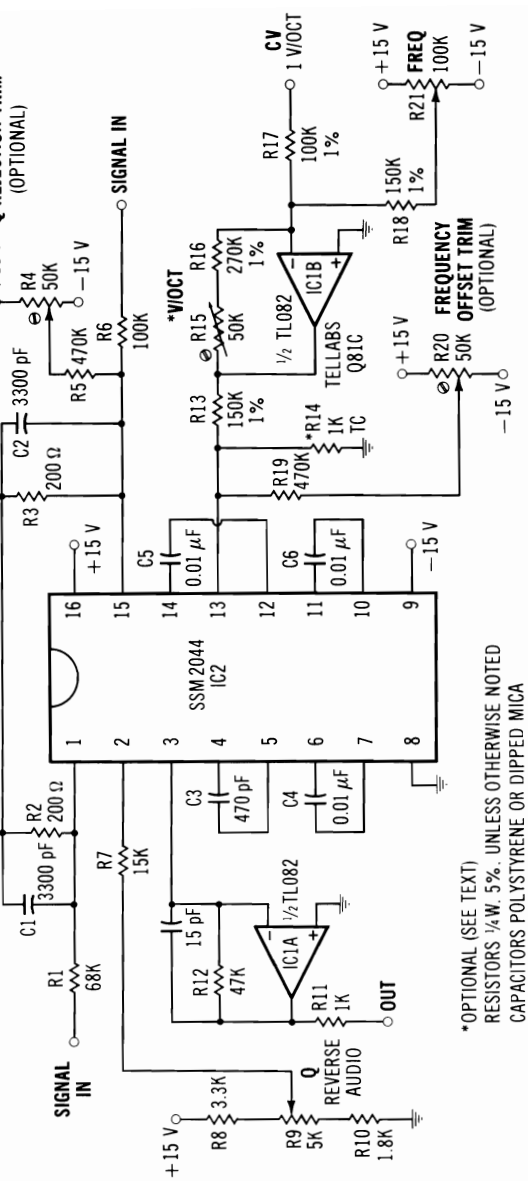



**Fig. 5-18. A vclpf using the SSM2044.**

signed so that the maximum peak-to-peak voltage at pin 13 will correspond to the maximum sweep range desired when the output of the op amp swings from supply rail to supply rail. This corresponds to ± 90 mV at pin 13 and a 1000-to-1 sweep range for ± 15-V supplies.

Fig. 5–19 is a block diagram of the Curtis Electromusic Specialties CEM3320 vcf IC. This IC contains an exponential current converter, four gain cell/buffer stages, and a variable transconductance cell useful for voltage controlled resonance. The gain cells are of a different design from typical transconductance cells (used in the SSM2040) in that they are current-in, current-out circuits (rather than voltage-in, current-out). Each cell is temperature compensated. The IC has a signal-to-noise ratio of 85 dB, low distortion, and can be configured for several filter structures.

The input to the CEM3320 gain cell is essentially a forward biased diode to ground. It is therefore a low-impedance sum-

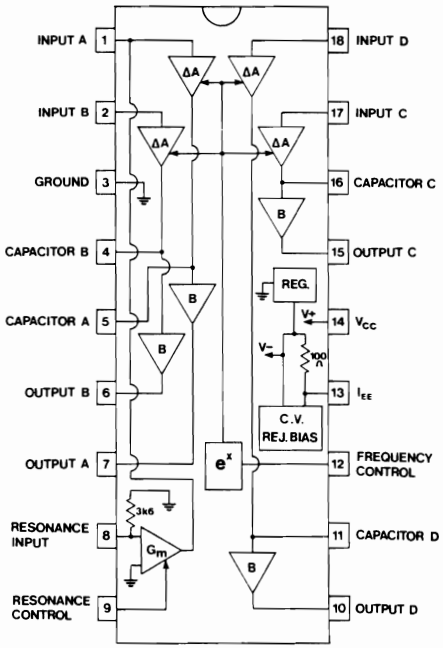



**Fig. 5-19. The Curtis Electromusic Specialties CEM3320.**
*(Courtesy* ETI Magazine *and Digisound, Ltd.)*

ming node at a nominal 650 mV above ground. The required input currents are thus created with input resistors to this node. For dc stability and a constant reference current to bias the input diode, a feedback resistor is connected from the buffer output to the summing node. The output current of the gain cell is given by the formula

$$I_{out} = (I_{ref} - I_{in})A_{I0}\exp(-V_C/V_T)$$

where

$V_T = KT/q$,
$V_C$ = voltage applied to pin 12,
$A_{I0}$ = current gain at $V_C = 0$ (nominally 0.9),
$I_{ref} = (0.46V_{CC} - 0.65\text{ V})/(10^5\ \Omega \pm 25\%)$.

A four-pole vclpf circuit using the CEM3320 is shown in Fig. 5–20.[1] Op amp IC1 attenuates the input signal and feeds it into the CEM3320 through C2 and R5. Capacitor C2 is necessary to maintain the required dc input bias to the first gain cell, set by feedback resistor R6. For minimum control voltage feedthrough and maximum peak-to-peak signal output, the buffer output voltage should be

$$V_{odc} = 0.46V_{CC}$$

which is 6.9 V for ± 15-V supplies. The feedback resistor for this circuit is calculated:

$$R_f = \frac{V_{odc} - 0.65\text{ V}}{I_{ref}} = \frac{6.9\text{ V} - 0.65\text{ V}}{6.25\text{ V}/10^5\ \Omega} = \frac{6.25\text{ V}}{63\ \mu\text{A}} = 99.2\text{ kilohms}$$

or 100 kilohms.

The output impedance of the gain cell has a finite value and looks like an ac resistance of 1 megohm in parallel with the feedback resistor $R_f$ (100 kilohms) to the input. The pole frequency of each stage is determined by the total equivalent feedback resistance ($R_{eq}$) and the pole capacitor $C_p$ as

$$f_p = A_{I0}\exp(-V_C/V_T)/2\pi R_{eq}C_p$$

where

$R_{eq} = (R_f \times 1\ M\Omega)/(R_f + 1\ M\Omega)$,

$A_{I0}$ = current gain at $V_C = 0$ (nominally 0.9),

$V_C$ = voltage applied to pin 12.

For subsequent filter stages the input current will be a sum of the currents from the feedback resistor and the current developed across the storage capacitor from the previous stage. This current will exceed the desired level; thus it is necessary to sink a portion of it with a resistor connected to the negative supply (as done with R9 on pin 2). This method maintains unity gain for stages 2, 3, and 4.

To control the resonance of the filter, a current of between 0 and 100 $\mu$A is sent to pin 9. An input current of 100 $\mu$A into pin 9 will cause the filter to oscillate. Resistor R28 was chosen for oscillation to occur at a 10-V input level. The resonance circuit is such that high voltages (input currents) will have less effect on the resonance. This gives us more control near the critical point of oscillation. Increasing the resonance control voltage above the level causing oscillation will increase the oscillation level and shift its frequency.

Minimization of control voltage feedthrough is obtained by adjusting trimmer R25. To adjust R25, alternate the minimum and maximum control voltages into IC3A and adjust R25 for the minimum change in the dc output level at pin 10. Trimmer R34 adjusts for a quiescent output voltage of 0 V. Optional $Q$ control voltage feedthrough trim is done with resistors R37 and R38 in a manner similar to the control voltage feedthrough adjustment instructions just mentioned.

The filter frequency control voltage should be between −25 mV and +155 mV at pin 12 for best results. Trimmer R22 adjusts for an 18-millivolt-per-octave frequency scaling. As the voltage input of IC3A becomes more positive, the cutoff frequency will rise. Resistor R27 sets the quiescent operation point of the filter at about 20 Hz.

### Voltage-Controlled All-Pass (Phase Shifting) Circuits

The phase shifter has become a very popular signal modification device for guitar and keyboard players. A circuit that has been used in these applications is shown in Fig. 5–21A. The basic shifter stage is shown in Fig. 4–21B. One notch in

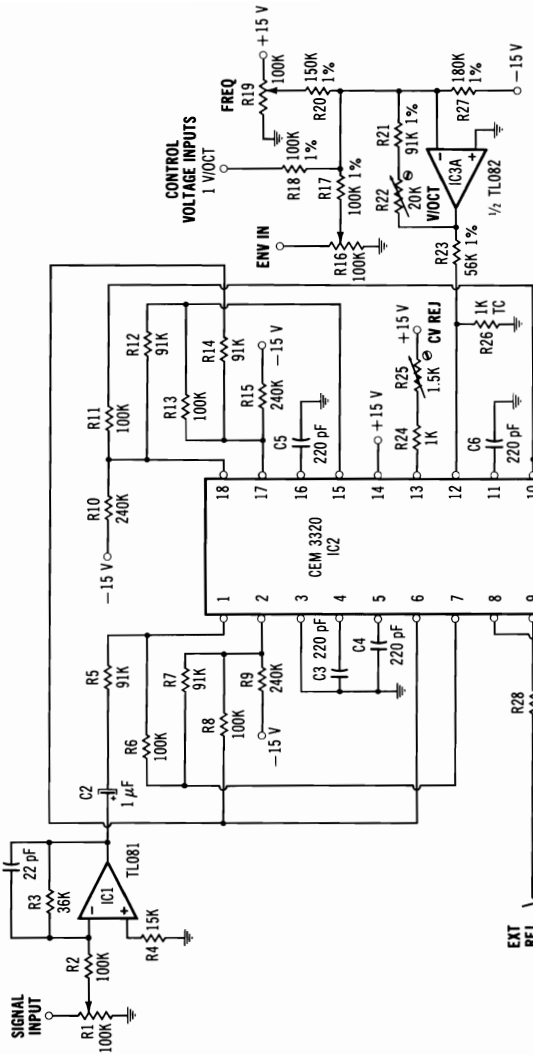
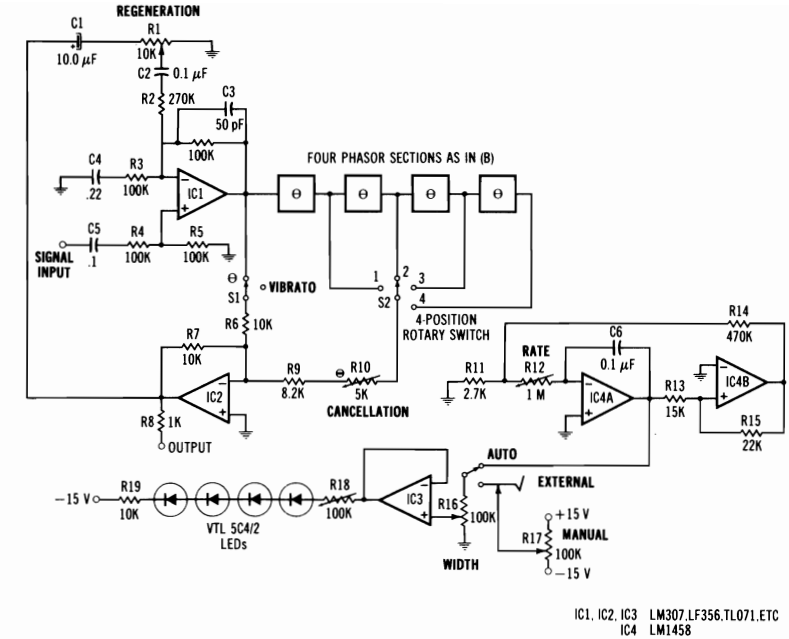
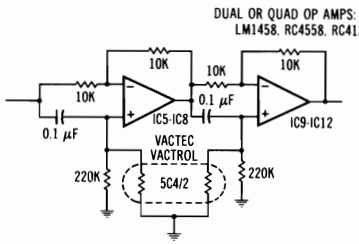



**Fig. 5-20. A vclpf using the CEM3320 vcf IC.**




(A) Phase shifter circuit.




(B) Phase shift section (creates one notch.)

**Fig. 5-21. A phase shifter circuit using Vactec "Vactrols."**

the frequency response will be created by each stage shown (thus 4 notches for this circuit). A Vactec "Vactrol" (a combination photocell/LED) is used in the phase shift sections to reduce the resistance of the 220-kilohm resistors, with the application of a control signal to the Vactrol's LED. As the brightness of the LED increases, the resistance of the internal photocell decreases. These photocells are relatively slow to react to decreases in the light level. This causes less variation in fre-

quency sweep with fast sweep rates. However, this is not objectionable—it is often preferable. The 0.1-$\mu$F capacitors shown in the shifting networks are chosen for phasing action in the lower frequencies. Some users may prefer a higher value, such as 0.01 $\mu$F. The phase shifter sounds best if all of these capacitors are of the same value.

The setting of switch S1 determines if the circuit acts as a phaser or a vibrato. With S1 open the circuit will be a vibrato since the signal is being shifted in time (phase). With S1 closed the shifted signal is compared with the unshifted signal, creating notches in the frequency response where the two signals are 180° apart. Switch S2 switches between phase stages. As the number of phase stages increases, so do the number of notches. A variation in the control voltage will shift these notches up and down the frequency spectrum. Trimmer R10 (near IC2) is adjusted for optimum notch depth. The regeneration control (R1 near IC1) feeds the output signal back to the input, thus increasing the intensity of the effect.

A lot of experimentation can be done with this circuit. For example, the source of regeneration can originate from the phase shifting circuitry (connect regen pot to wiper of S2) before being summed with the "clean" signal at IC2. The number of phase shift sections can be increased. Peaks will be created in the frequency response (instead of notches) if the shifted output is inverted before being summed with the clean signal. Also, the circuit is designed for unity gain. If lower-level signals are to be used (such as those from a guitar) a better signal-to-noise ratio will be obtained if the gain of IC1 is increased, causing a larger signal to pass through the shifting circuit. The output and the clean signals are then attenuated as they are mixed by using larger values for resistors R6 and R9. Notice that increasing regeneration will increase the signal level (or even cause oscillation). Therefore you will have to leave some headroom for this increase in signal level throughout the circuit.

Fig. 5–22 contains a two-notch, voltage controlled, all-pass circuit using the CEM3320.[2] Much of the control circuitry is similar to that in the vclpf circuit seen previously (Fig. 5–20).

Fig. 5–23 contains a voltage controlled, all-pass/low-pass filter using the SSM2040. An all-pass response (two notch) is achieved by switching all the capacitors to the previous stage. Grounding the capacitors as shown will produce a four-pole,

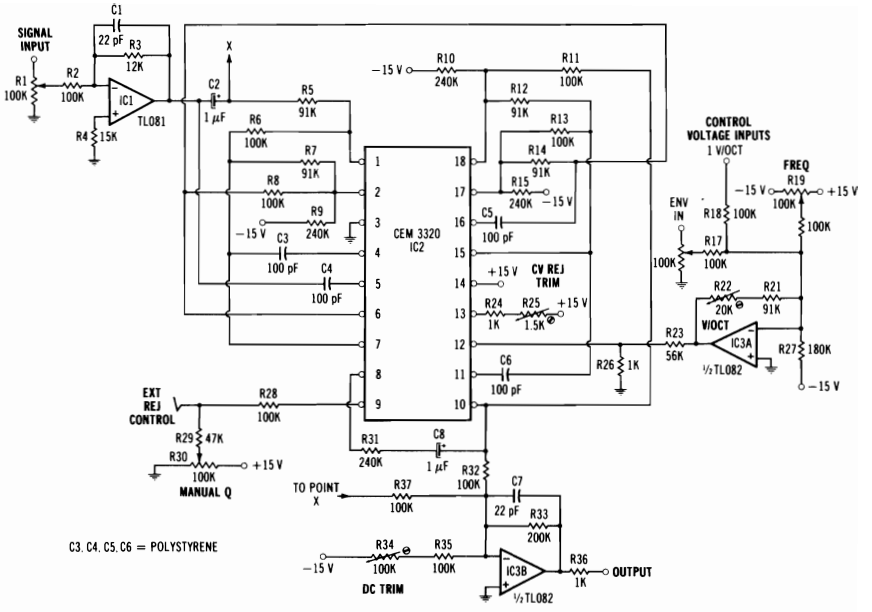
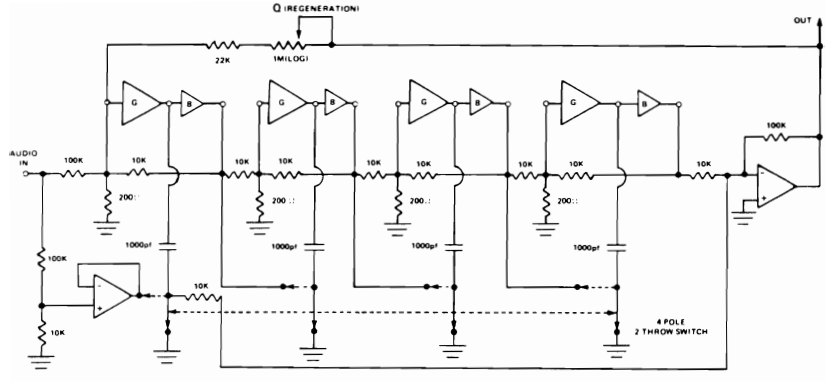


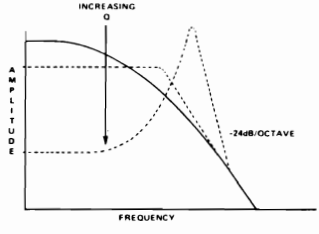

**Fig. 5-22. A two-notch all-pass filter using the CEM3320.**
*(Courtesy* ETI Magazine *and Digisound Ltd.)*

low-pass response. Some interesting effects can be obtained if individual switches are used rather than the four-pole, double-throw switch shown. This will enable mixing all-pass and low-pass responses for new timbres. The control voltage circuitry used in the SSM2040 vclpf circuit of Fig. 5–15 (IC1) can be used to drive the control voltage input pin (pin 7) of the SSM2040. You may wish to try raising the pole frequency capacitor values from 0.001 $\mu$F to 0.002 $\mu$F or so for increased response in the lower frequency ranges.

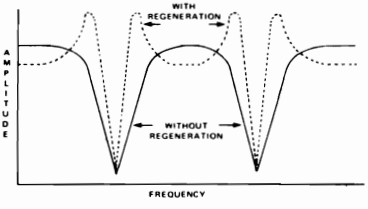
Although it is fairly simple to design all-pass circuits with custom vcf chips as we have seen, there is some question as to whether the simple 2-notch response is worth the cost. This simple response is typical of inexpensive phase shifters. It would be nice to have a circuit with more notches, one similar to the circuit of Fig. 5–21. Fig. 5–24 contains a simple current controlled, phase shift circuit that can be cascaded as in Fig. 5–21 to produce a phase shifter circuit with many notches. Remember, however, that since these stages are cascaded, circuit




(A) Circuit.




(B) 4-pole low-pass filter response.




(C) 4-pole phasor response.

**Fig. 5-23. A combination phasor/low-pass filter using the SSM2040.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

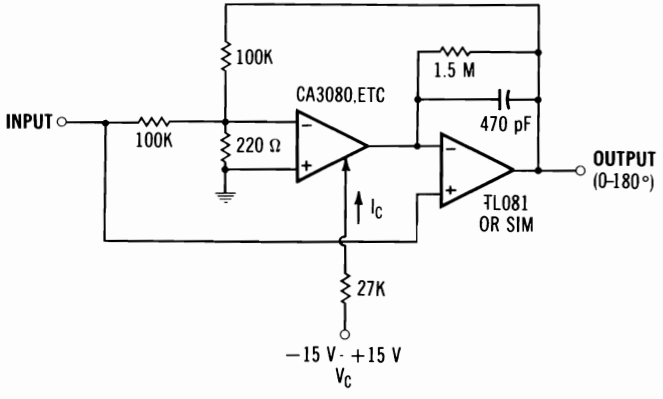


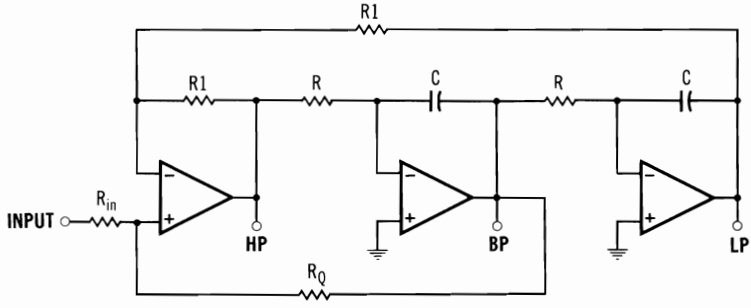

**Fig. 5-24. A voltage controlled phase shift network using an ota.**

noise increases as more stages are added. The use of the new dual ota's with linearized inputs will reduce this problem somewhat.

### State-Variable Filters

The *state-variable* filter (sometimes called a *universal active* filter) is a filter that provides low-pass, bandpass, and high-pass responses simultaneously. The basic configuration is shown in Fig. 5–25. This circuit will have 12 dB per octave high- and low-pass responses and a second-order bandpass response. The high- and low-pass outputs are 180° out of phase. Combining these two outputs will give a notch response. This type of response, however, is not very useful, as it is hard to notice any difference in the sound unless the notch is fairly wide. Controlling this type of filter with a variable voltage is accomplished using voltage controlled integrators for these two outputs.

A voltage controlled state-variable filter using ota's appears in Fig. 5–26.[3] Emitter follower Q1 sets the minimum output current for the exponential current converter circuit at 100 $\mu$A. The collectors of Q2 and Q3 must go to a point more negative than their emitters to enable them to source current. The maximum limit of this current will be set by resistors R13 and R14 (15 V/18 k$\Omega$ = 0.83 mA). The maximum value of this current will




$$f_c = \frac{1}{2\pi RC}$$

$$Q = \frac{R_{in} + R_Q}{2R_{in}}$$

$$R_Q = R_{in}(2Q - 1)$$

$$\text{BANDPASS OUTPUT GAIN} = \frac{R_Q}{R_{in}}$$

$$\text{LOW-PASS/HIGH-PASS GAIN} = \frac{2R_Q}{R_{in} + R_Q}$$

**Fig. 5-25. The state-variable filter.**

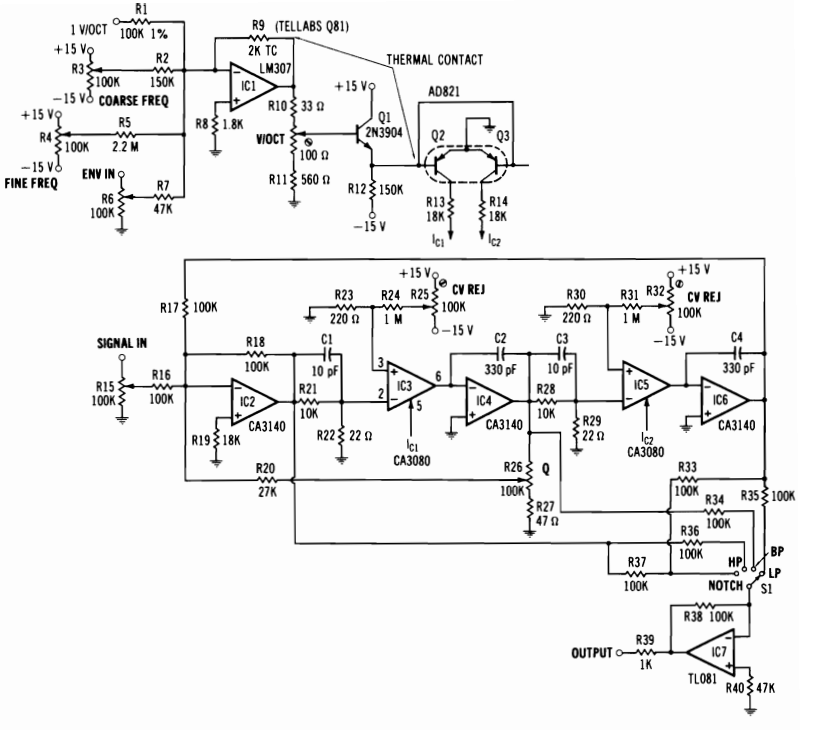



**Fig. 5-26. A voltage controlled state-variable filter using ota's.** *(Courtesy* Electronotes*)*

decide the upper-frequency cutoff of the circuit. A matched transistor pair is used for Q2 and Q3 to guarantee equal driving currents for the ota's. For less critical applications of this filter, these transistors can be two 2N3906s and the 2-kilohm positive temperature coefficient resistor can be replaced with a 5-percent carbon resistor. CA3140s are used in this circuit for their low bias current requirements. These op amps cannot drive low-impedance loads (less than 2 kΩ). This is why an output buffer/summing amplifier, IC7, is included.

The CA3140 op amps may be replaced with another type of FET-input op amp that can drive low-impedance loads. This can eliminate the need for IC7. However, there may be some loss in performance (changes in the maximum value of $Q$ and the low-frequency cutoff limit). A constant $Q$ is maintained over

the full range of frequencies by capacitors C1 and C3 (on the outputs of IC2 and IC4, respectively). These provide a phase lead for high frequencies, making up for phase lag caused by the internal circuitry of the ICs.

To determine the high-frequency cutoff for this circuit, we must know the formula for the ota output current. For the CA3080 this is

$$I_{out} = 19.2\, I_C V_{DI}$$

where

$I_{out}$ = output current in amperes,
$I_C$ = control current in amperes,
$V_{DI}$ = differential voltage, in volts, between ota inputs.

Since we are typically using a ± 5-V signal and have a 10-kilohm: 22-ohm attenuator on the ota input, $V_{DI}$ can be found by

$$V_{DI} = \frac{22\, V_{in}}{10\,000} = 0.011 \text{ V or } 11 \text{ mV} \qquad (V_{in} = 5 \text{ V})$$

$$\begin{aligned} I_{out} &= 19.2\, I_C\ (0.011 \text{ V}) \\ &= 0.211\, I_C \\ &= 0.211 \times 0.83 \text{ mA (maximum output current)} \\ &= 0.175 \text{ mA} \end{aligned}$$

This output current is then converted to an equivalent resistance:

$$R_{eq} = \frac{V_{in}}{I_{out}} = \frac{5}{0.175} = 28.6 \text{ k}\Omega$$

The formula for the frequency cutoff in kilohertz is

$$f_c = \frac{1}{2\pi RC} = \frac{1}{6.28 \times 28.6 \text{ k}\Omega \times 330 \text{ pF}} = 16.9 \text{ kHz}$$

Trimmers R25 and R32 are for adjusting the rejection of the control voltage by the filter. Initially they are set to their mid-

range and then each is adjusted for a minimum output dc shift, while the coarse frequency control is varied over its full range.

A similar state-variable design using the SSM2040 is shown in Fig. 5–27.[4] In this circuit two second-order state-variable filters are cascaded to form a fourth-order filter. Switch S1 will switch between 12 and 24 db-per-octave responses for the various filter responses. Since the SSM2040 does not have on-chip voltage controlled resonance, an LM13600 is used in the "front end" of the filter. The signal input to this filter should not exceed 10 V peak to peak. The voltage control circuitry of IC5A should be familiar to you by now. If desired, a positive temperature coefficient resistor can be substituted for R47 on the output of IC5A. Trimmers PR1 and PR2 must be adjusted to obtain the correct filter responses. Initially, set them to their midrange and monitor the BP2 output. Adjust PR1 until an abrupt change from a low-pass response to a bandpass response is heard. Leave PR1 at this setting. Then monitor the LP4 output and adjust PR2 for a low-pass response at the output. Refer to Fig. 5–4 for more precise adjustment of these trimmers.

This filter is not designed to oscillate at high $Q$. Therefore the 1 V/OCT trimmer can be adjusted in one of two ways. The first is to monitor the voltage at IC1, pin 7, for an 18-mV increase for every 1 V increase in control voltage. The second method is to track a calibrated sine wave vco that used an identical control voltage. Adjust the control voltage (to the vcf and vco) for a vco frequency of about 250 Hz. Adjust the filter frequency controls for a peak in the bandpass output amplitude. Then increase the control voltage (to both vco and vcf) 1 volt and adjust trimmer PR3 for a peaking in the bankpass output amplitude.

Fig. 5–28A contains a voltage controlled state-variable filter using the CEM3320. This circuit is similar to the last one, except some changes are necessary because of the 6.9-V offsets of the gain cells. An LM13600 is used to provide voltage controlled resonance. Its input is ac coupled to prevent level shifting of the CEM3320 gain cell. Op amps (IC2–IC5) are necessary for buffering the filter outputs and level shifting for a ground-referenced output signal. The circuit shown is a second-order filter. To obtain a fourth-order response, it is necessary to casade two filter circuits as shown in Fig. 5–28B. (This is the same scheme used with the SSM2040.)

Unfortunately, this design requires a lot of external parts (op

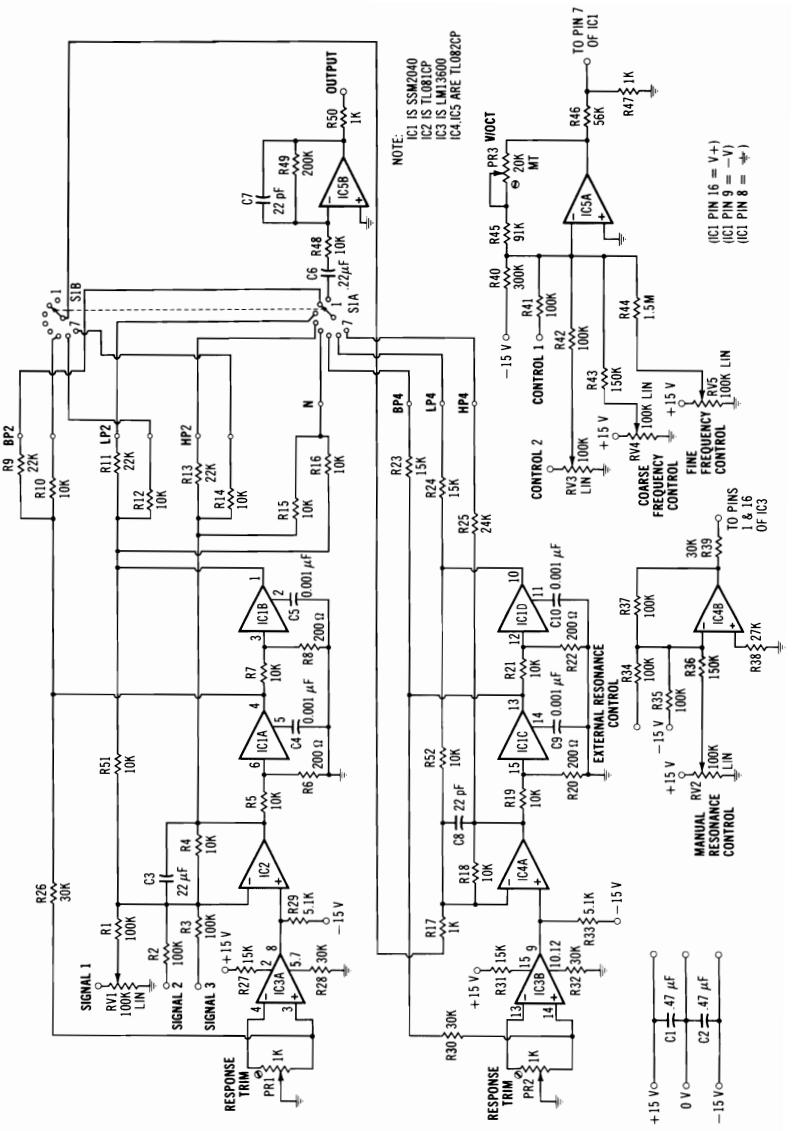
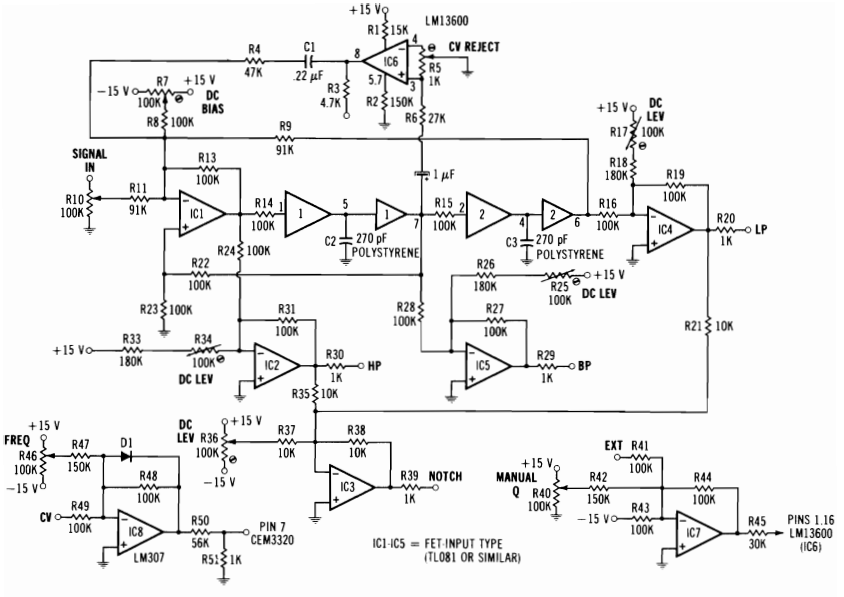
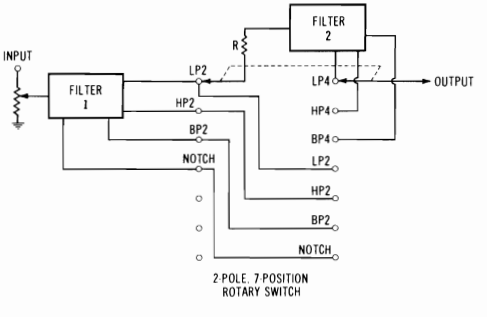



**Fig. 5-27. A voltage controlled state-variable filter using the SSM2040.**
*(Courtesy* ETI Magazine *and Digisound, Ltd.)*



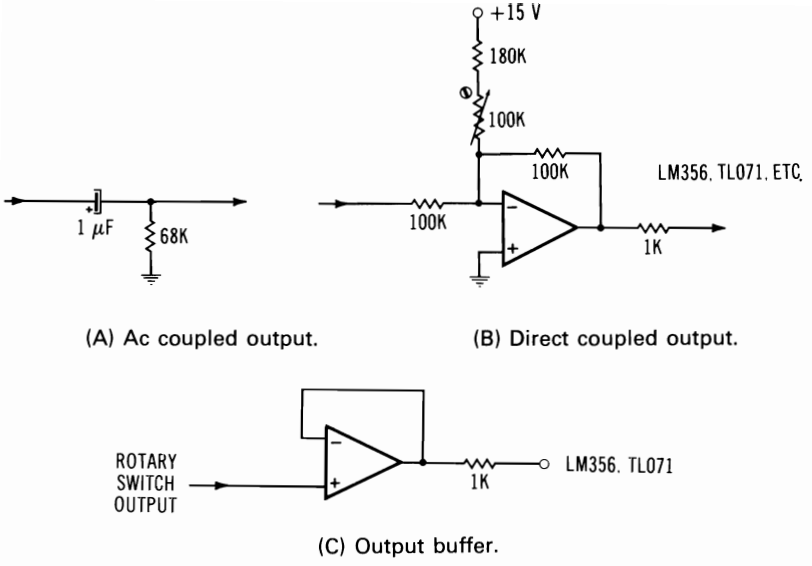

(A) Circuit.




(B) Cascaded filter circuits.

**Fig. 5-28. A voltage controlled state-variable filter using the CEM3320.**

amps, trimmers, etc.). If you wish to build a fourth-order circuit with the CEM3320, you might try ac coupling the outputs of the filter sections as shown in Fig. 5–29A. This will eliminate several op amps and trimmers. The notch output circuit will have to remain unchanged, however, to prevent signal attenuation




(A) Ac coupled output.

(B) Direct coupled output.

(C) Output buffer.

**Fig. 5-29. Output coupling methods for the circuit of Fig. 5-28.**

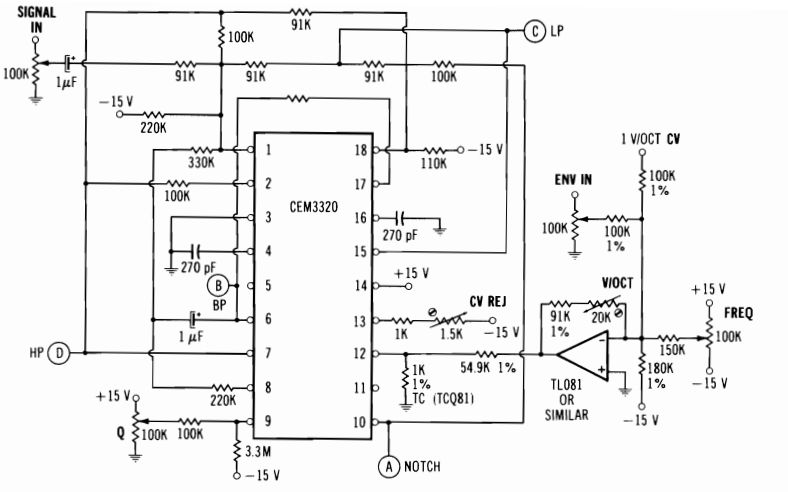
that would be caused by the 68-kΩ resistor. Also, an op amp will be required to buffer the output of the rotary switch.

If you are satisfied with just a second-order response, the circuit in Fig. 5–30 can be used. This circuit uses two of the gain cells as inverters. The voltage controlled resonance gain cell is used in this circuit.

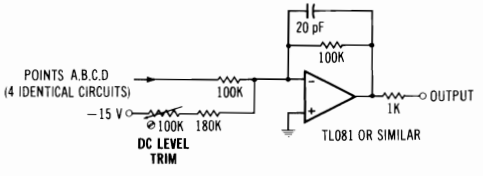
A very interesting IC recently introduced is the Curtis Electromusic Specialties CEM3350 dual voltage-controlled state-variable filter. This IC contains two independent state-variable filters in a 16-pin dip package. A block diagram of the IC appears in Fig. 5–31. Each filter has its own set of frequency and $Q$ control inputs. Both frequency and $Q$ control inputs transform a linear voltage into an exponential control function. The filter frequency can be controlled over a 15-octave range. The $Q$ can be controlled from ½ to a value of 100.

The gain cells used in the CEM3350 are of the standard variable-transconductance (ota) type. Their maximum input level (before excessive distortion) is 50 mV peak to peak. This means an input attenuator will be required to work with ± 5-V signals.

An interesting feature of this IC is the choice of inputs pro-




(A) Circuit.

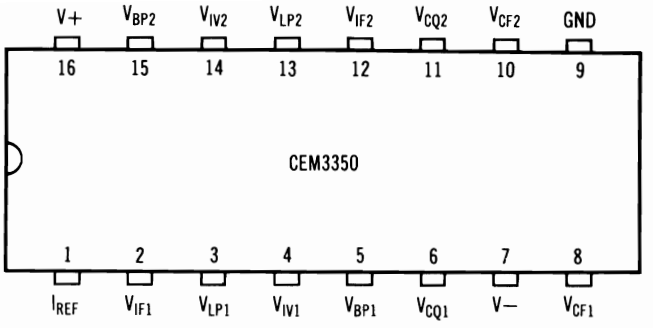



(B) Points A, B, C, and D (four identical circuits).

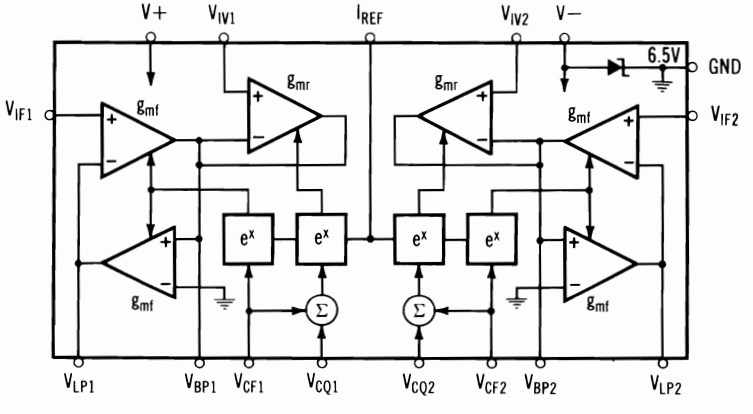
**Fig. 5-30. A second-order state-variable filter using the CEM3320.**
*(Courtesy Curtis Electromusic Specialties)*

vided for each section. For signals applied to the "fixed" input (pins 2 and 12), the signal amplitude in the filter passband will remain constant (50 mV p-p) as the $Q$ is varied. However, the amplitude at the filter cutoff frequency will peak higher than the passband amplitude as $Q$ is increased. For some applications the input signal will have to be reduced in amplitude to prevent a curious amplitude "jump" that occurs as the signal frequency approaches the filter cutoff frequency. This jump in amplitude occurs because the increased amplitude at $f_c$, due to the high $Q$, overloads the gain cells in the filter.

A second input, called the "variable" input, limits the amplitude at the filter cutoff frequency to 50 mV and at the




(A) Pin diagram.




(B) Block diagram.

**Fig. 5-31. The CEM3350 dual state-variable vcf.**
*(Courtesy Curtis Electromusic Specialties)*

same time reduces the filter passband amplitude as the $Q$ is increased.

The input signal can be summed into both these inputs to simulate additional filter responses. A four-pole, low-pass filter using this method is shown in Fig. 5–32. Note that this is the traditional cascaded, first-order, low-pass circuit as seen previously. The current output of each gain cell is fed into a capacitor. The voltage developed across the capacitor is sensed by the input of the next gain cell. The voltage across the last

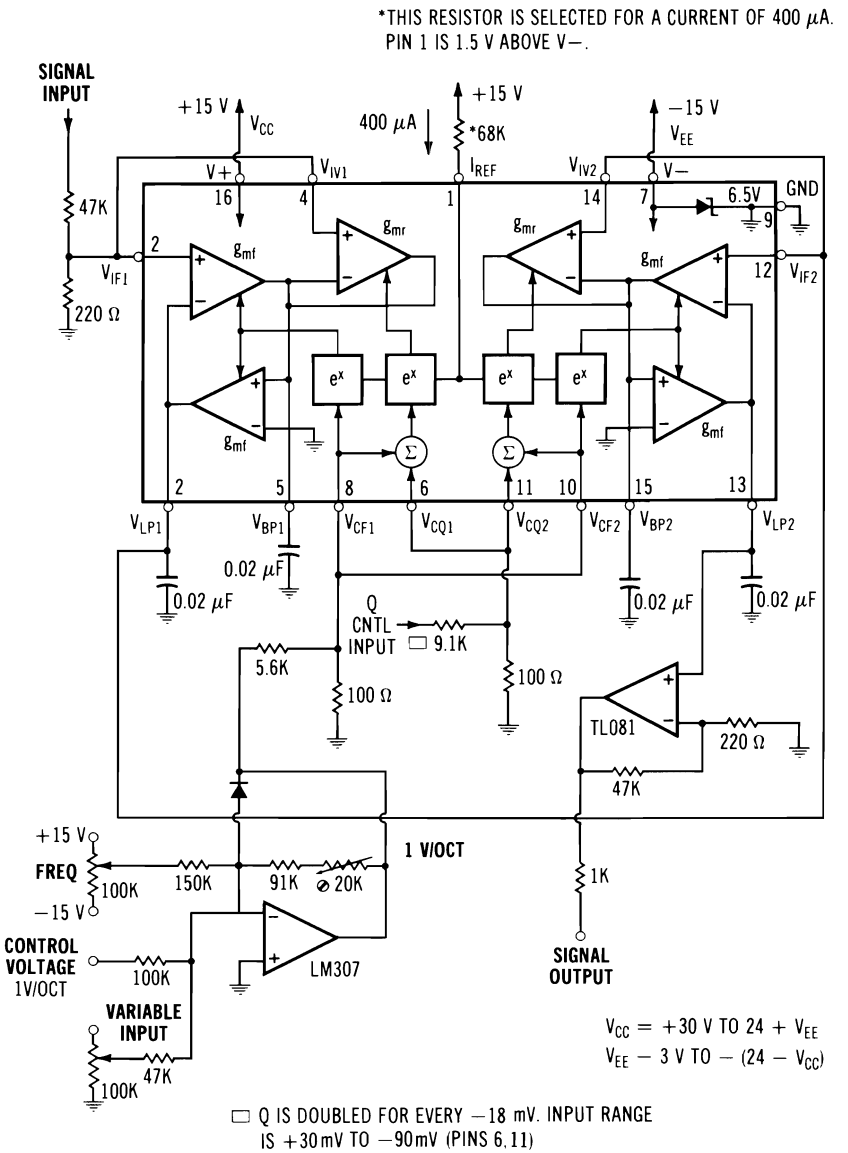



**Fig. 5-32. A four-pole, voltage controlled, low-pass filter using the CEM3350.**

capacitor is buffered and amplified by an op amp for the final output.

Fig. 5–33 illustrates the required connections for two independent state-variable filters. Note that for each filter only two of the three possible responses are available at a time. The normal outputs are the low-pass and the bandpass. By feeding the input through a capacitor as shown, however, these switch to bandpass and high-pass, respectively. The diode networks shown in the schematic will reduce $Q$ at large signal levels, thereby eliminating the amplitude jump problem discussed earlier.

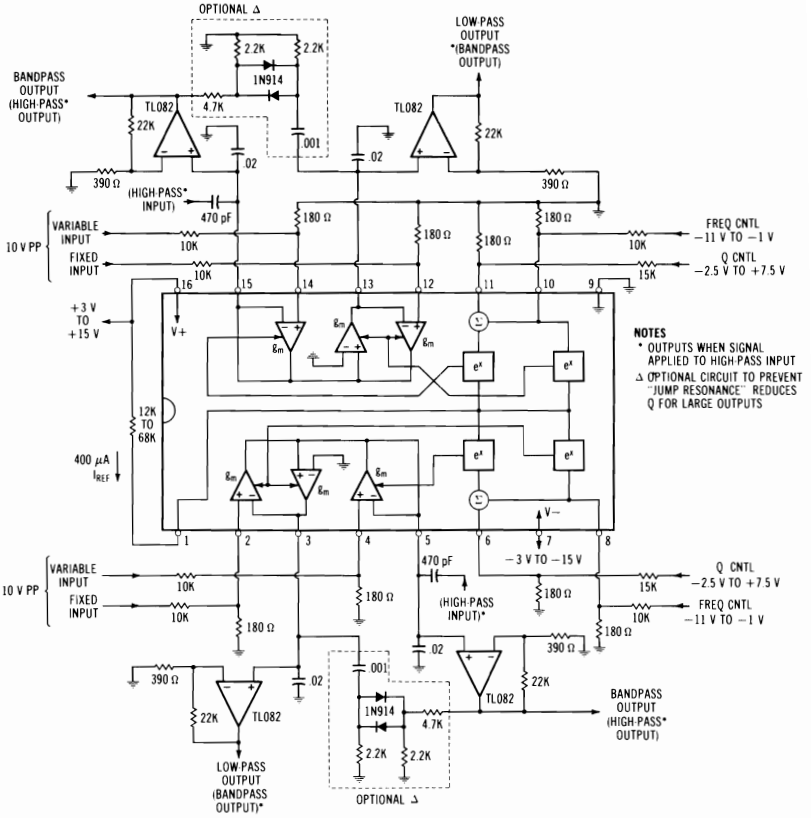



**Fig. 5-33. Basic circuit connections for the CEM3350 dual state-variable filter.** *(Courtesy Curtis Electromusic Specialties)*

The frequency control input is meant to work with the now familiar inverting summing stage common to other circuits in this chapter. The control voltage range *into pin 8 or pin 10* is −200 mV to 0 mV. The scale is the standard −18 mV per octave. The $Q$ control input (pin 6 or pin 11) control range is +30 mV to −90 mV. The $Q$ increases by a factor of 2 for every −18 mV.

## FIXED FILTER CIRCUITS

Now let us look at two types of fixed filters: the graphic equalizer and the vocoder.

### The Graphic Equalizer

A *graphic equalizer* consists of several bandpass circuits which can be used to boost or attenuate portions of the audio spectrum. It is often used as a final equalizer for a synthesizer, much like a studio mixing board equalizer is used. The design of a graphic equalizer can be attempted by designing a bank of two- (or more) pole, active bandpass filters or using the approach shown in Fig. 5–34.[5] In this design, resonant networks are created with inductors (or simulated inductors, as we shall see) to boost or cut frequencies as desired. In Fig. 5–35 active circuitry is used to simulate the inductor used in Fig. 5–34.[6] Additional design information can be found in National Semiconductor's *Audio/Radio Handbook*.

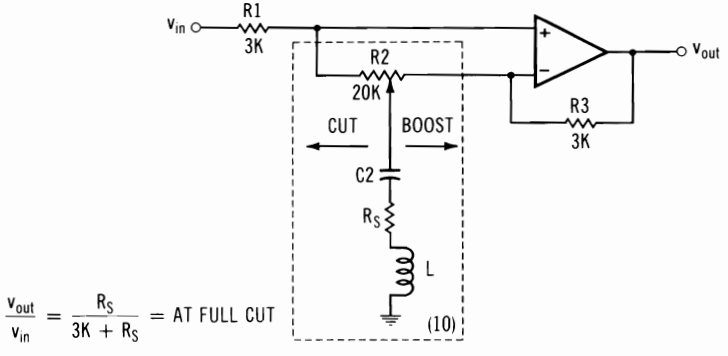
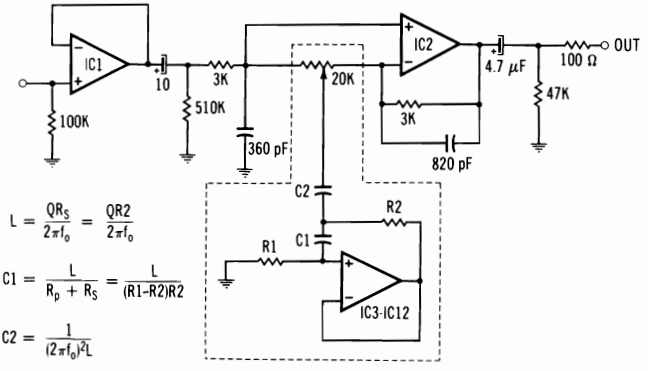
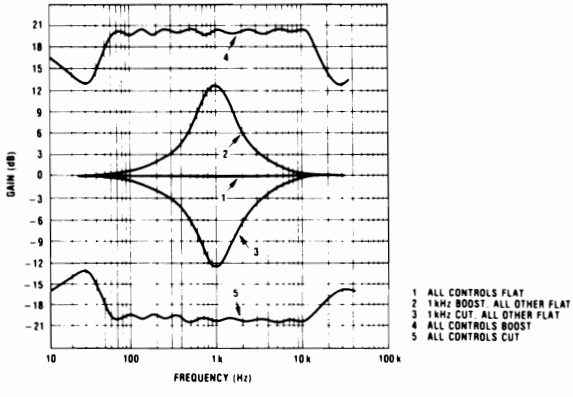



**Fig. 5-34. A graphic equalizer using an inductor.**
*(Courtesy National Semiconductor Corp.)*




(A) Circuitry.


GAIN (dB)
FREQUENCY (Hz)
1 ALL CONTROLS FLAT
2 1kHz BOOST. ALL OTHER FLAT
3 1kHz CUT. ALL OTHER FLAT
4 ALL CONTROLS BOOST
5 ALL CONTROLS CUT

(B) Response.

| fo(Hz) | $C_1$ | $C_2$ | $R_1$ | $R_2$ |
|---|---|---|---|---|
| 32 | 0.12μF | 4.7μF | 75kΩ | 560Ω |
| 64 | 0.056μF | 3.3μF | 68kΩ | 510Ω |
| 125 | 0.033μF | 1.5μF | 62kΩ | 510Ω |
| 250 | 0.015μF | 0.82μF | 68kΩ | 470Ω |
| 500 | 8200pF | 0.39μF | 62kΩ | 470Ω |
| 1k | 3900pF | 0.22μF | 68kΩ | 470Ω |
| 2k | 2000pF | 0.1μF | 68kΩ | 470Ω |
| 4k | 1100pF | 0.056μF | 62kΩ | 470Ω |
| 8k | 510pF | 0.022μF | 68kΩ | 510Ω |
| 16k | 330pF | 0.012μF | 51kΩ | 510Ω |

(C) *R* and *C* values.

**Fig. 5-35. A graphic equalizer using op amps as simulated inductors.** *(Courtesy National Semiconductor Corp.)*

## Vocoders

An interesting device using two sets of fixed filter banks is the *vocoder*. Fig. 5–36 is a block diagram of a vocoder system. A vocoder uses one bank of high-$Q$ bandpass filters to frequency analyse the input signal. The output of each bandpass filter is connected to an envelope follower. The output of each envelope follower is used as a control voltage to a voltage controlled amplifier that follows another identical high-$Q$ bandpass filter. This second bank of bandpass filters is fed a different input signal. The net effect is that the timbre of the first bank of filters will control the timbre of the second bank. This leads to some bizarre sound effects.

Due to the complexity of a typical vocoder system it can hardly be termed a synthesizer module. Some useful effects, however, can be experienced with fewer filter sections. If you are thinking of designing a large vocoder system the following two references can help you out:

*ETI Magazine*, September, 1980:
14-band unit with timbre "freeze" switch and slew rate control (kit available from Powertran, Portway Industrial Estate, Andover, HANTS SP10 3NM, Hampshire, England).

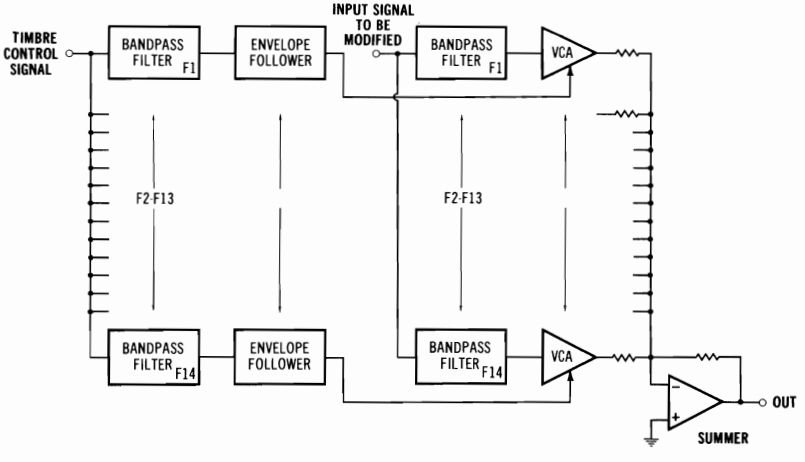


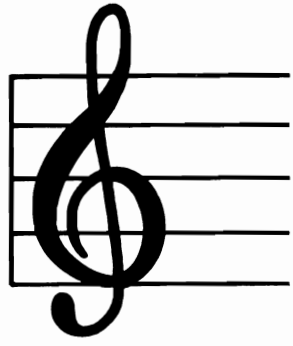

**Fig. 5-36. Block diagram of a vocoder.**

*Electronotes*, No. 100: 16-band unit using state-variable filters.

## REFERENCES


1. *ETI Magazine*, Vol. 9, No. 5, May 1980, pp. 20–25.
2. *ETI Magazine,* Vol. 9, No. 5, May 1980, pp. 20–25.
3. Hutchins, Bernie, "The ENS-76 Home Built Synthesizer System—Part 5," *Electronotes,* No. 71, November 1976, pp. 14–18.
4. *ETI Magazine,* Vol. 9, No. 7, July 1980, pp. 84–87.
5. National Semiconductor Corp., *Audio/Radio Handbook.* 1980, pp. 2–59 through 2–61.
6. Ibid.

# ANALOG MULTIPLIERS



# CHAPTER 6

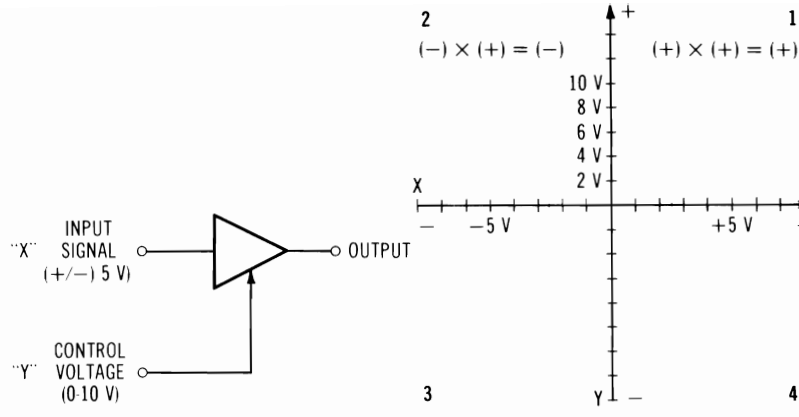
*Analog multipliers* are circuits that multiply the instantaneous voltage of an input signal by the instantaneous voltage of another input signal or control signal. The most common analog multiplier is the *voltage controlled amplifier*, or *vca*. A vca has a signal input and a control voltage input. The signal input usually accepts bipolar (+/−5 V) signals and the control voltage input accepts only unipolar (0 to 5 or 10 V) voltages. Voltage controlled amplifiers of this type are often called *two-quadrant multipliers* because the algebraic sign of the product (or output of the circuit) can fall in either of two quadrants (quadrants 1 and 2) of a four-quadrant graph, as shown in Fig. 6–1.

The output of the vca is scaled so that unity gain appears at the output when the control voltage is at its maximum. For instance, if you were using +/−5-V signal levels and a 0- to 5-V control voltage, the output would be scaled to XY/5 for unity gain. The output of the vca will be zero as the control voltage reaches or goes more negative than 0 V.

Voltage controlled amplifiers are often one of the last modules in a system patch. Generally, a vca accepts a control voltage from an envelope generator that is triggered by the keyboard.

The gain of a vca is linearly and/or exponentially controlled. Most vca's have linear control inputs. Operation under exponential control results in a more abrupt change in output amplitude in response to the control voltage.

Another type of analog multiplier is the *balanced modulator*,




(A) Circuit. (B) Product falls in quadrant 1 or 2.

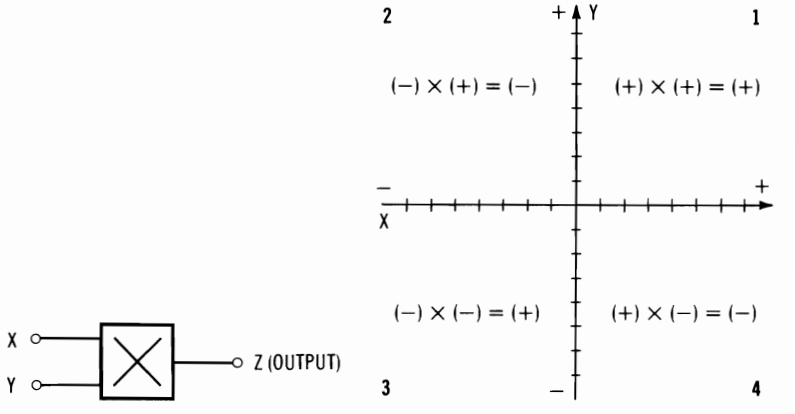
**Fig. 6-1. The algebraic product of a vca.**

or *ring modulator*. This type of multiplier accepts bipolar signals on both inputs. For this reason, either input can be considered the control input—there is no distinction between a signal and a control voltage. The output can appear in any one of the four quadrants, as shown in Fig. 6–2. For this reason, such a circuit is often termed a *four-quadrant multiplier*. The balanced modulator can be used as a vca but the output voltage will be zero only when the control (or signal) input is exactly 0 V. Also, the range of amplitude control of a balanced modulator is usually not as great as a two-quadrant multiplier. Balanced modulators are generally used for generating complex timbres by multiplying two audio signals. This results in frequency "sidebands" created at the sum and difference frequencies of the two input signals. This phenomenon is often used to create bell sounds.

Balanced modulators can be designed using 2 two-quadrant multipliers or a special purpose four-quadrant multiplier IC. In either case, precise trimming of the circuit is usually required for acceptable performance.

## TWO-QUADRANT MULTIPLIER VCA'S

We will now look at several types of two-quadrant multiplier vca's.




(A) Circuit.

(B) Product falls in quadrant 1, 2, 3, or 4.

**Fig. 6-2. The algebraic product of a balanced modulator.**

## Discrete VCAs

The heart of most vca designs is a variable transconductance amplifier (transconductance $g_m = \Delta I_{out}/\Delta E_{in}$). Before this became available in IC form (ota) it had to be constructed with discrete components. Fig. 6–3 contains a discrete vca using a CA3046 transistor array.[1] It consists of a differential amplifier (transistors Q1 and Q2) driven by a variable current sink (transistors Q3, Q4, Q5 and IC2). The inputs of the differential amplifier (+IN and −IN) will saturate with voltages approaching 100 mV. Up to this point the collector currents and the input base voltages will be exponentially related, as we have seen before. If the peak input voltage level is kept very small, say below 10 mV, distortion (due to the exponential function) is around 1 percent.

In Fig. 6–3 op amp IC1 also acts as a differential amplifier, sensing differences between collector currents and generating a voltage that corresponds to this difference. As the emitter currents are increased by the current sink the corresponding collector currents will increase and the magnitude of the difference between these two collector currents will also increase. This has the effect of varying the gain of the circuit.

Op amp IC2 and transistors Q3, Q4, and Q5 form a linear current sink for the differential transistor pair Q1 and Q2. Since the base-emitter voltages of transistors Q3 and Q4 are the same,

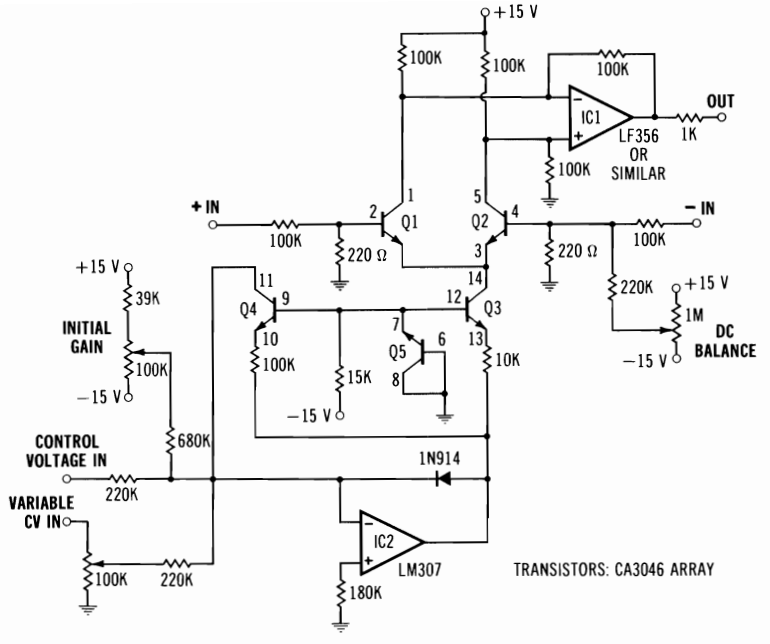


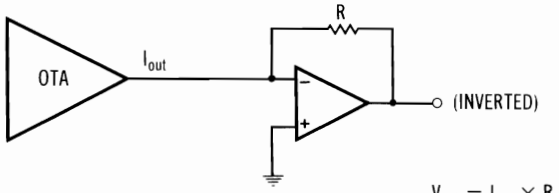

**Fig. 6-3. A discrete vca.**

their collector currents are identical. The current through Q4 is controlled by IC2. Transistor Q5 acts as a diode. It and the 15-kΩ resistor place a slightly negative voltage on the bases of Q3 and Q4 to prevent saturation. The diode in the feedback path of IC2 prevents negative control voltages from affecting the circuit.

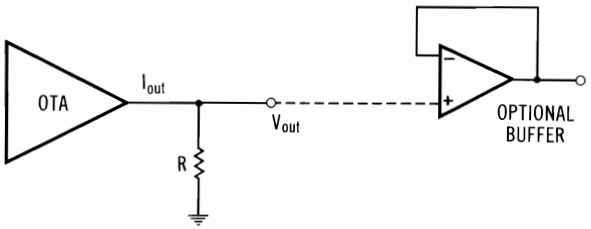
The gain of this circuit is temperature dependent, but since this effect is not generally audible, compensation is not necessary. The control range of this circuit is approximately 60 dB. This is not as high as we would generally like. A range of at least 70 dB is required for a decent signal-to-noise ratio.

## The OTA

The ota has become the workhorse of many gain control applications. As shown in the last chapter, the gain of the ota is controlled by varying the control current ($I_C$) of the amplifier. The output current is then converted to a voltage by a load resistor or current-to-voltage converter (Fig. 6–4). The internal




(A) Using load resister.




(B) Using current-to-voltage conversion.

**Fig. 6-4. Methods of current-to-voltage conversion.**

circuitry of the ota resembles the discrete circuitry of Fig. 6–3. Typically, voltage input levels must be less than 10 mV peak to peak to prevent excessive distortion. The dual ota's contain diode linearization networks that predistort the input signal in a manner opposite to the distortion generated by the ota, enabling input signals ranging up to 50 mV peak to peak to be used with acceptable distortion.

### The CA3080

The gain of the CA3080 is controlled by a current sourced into pin 5 (see Fig. 6–5[2]). The output current in amperes is

$$I_{out} = 19.2\, I_C V_{dif}$$

where

$I_C$ is the control current in amperes,

$V_{dif}$ is the voltage, in volts, between pins 2 and 3.

The CA3080 can have a maximum input voltage difference of 5 V. The maximum allowable control current is 2 mA. The device can operate on supplies up to ±18 V.

In Fig. 6–5 the +/−5-V input signal to the CA3080 is at-

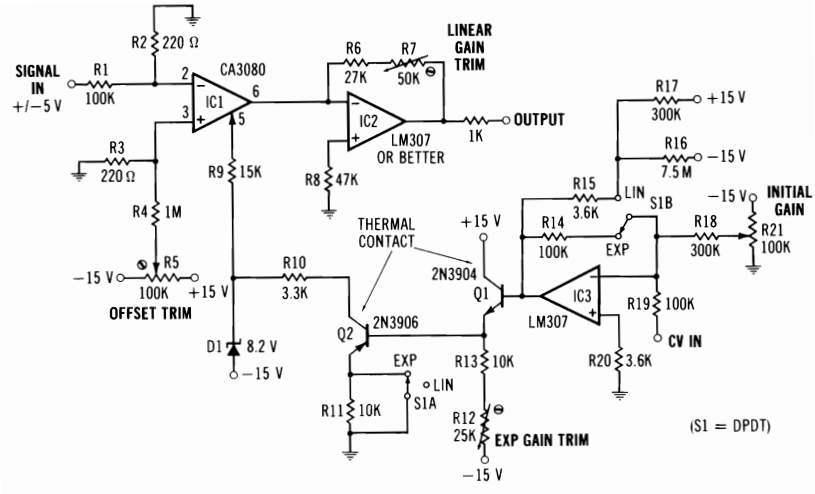



**Fig. 6-5. A linear/exponential control vca.**

tenuated to +/−11 mV by resistors R1 and R2. Trimmer R5 nulls out control voltage offsets in the 3080. This is adjusted for a minimum dc change in the output as the control voltage is varied. This circuit provides the option of either linear or exponential control as determined by the position of dpdt switch S1. Transistors Q1 and Q2 make up an exponential (current) converter when S1 is in the exponential mode. This vca has unity gain when the sum of the control voltages (INITIAL GAIN setting added with voltage present at CV input) is 5 V. To operate with a 0 to 10-V control range, double the value of R19. To adjust the gain of this circuit, set the wiper of R21 to ground and switch S1 to the linear mode. Using a +/−5-V sine wave, adjust the linear gain trimmer (R7) for unity gain. Switch to the exponential mode and adjust trimmer R12 for unity gain. This circuit has a dynamic range of close to 100 dB.

Fig. 6–6 shows a CA3080-based vca that accepts a linear control voltage, using a voltage controlled current source (op amp IC1).[3] In this circuit the summing node of IC1 sources current to the CA3080. The output of IC1 is connected to the negative supply pin of the 3080. The voltage at this pin will be 0.6 V (the voltage drop across D1) plus the required voltage level that provides a source current identical with the current through control voltage input resistors R1 and R5. This voltage (on pin 4

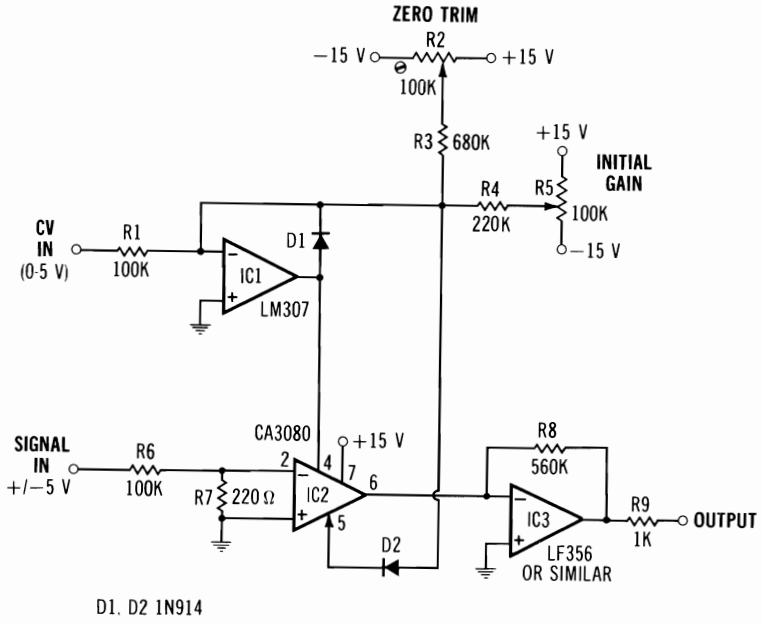



**Fig. 6-6. A linear control vca.**

of the CA3080) is about −1 V. Diode D1 prevents any negative control voltages from being inverted by IC1 to positive voltages, which would go to pin 4 of IC2. Trimmer R2 is used to adjust the vca output to 0 V with a control voltage of 0 V. This trimmer can be offset to cut short the exponential release time of a control voltage from an envelope generator. See Fig. 6–7.

## The CA3280

The CA3280 (RCA) is a dual ota containing diodes connected to the signal inputs that, if biased on, will allow increased input signal levels before distortion occurs (see Fig. 6–8A). If the diodes are biased off (diode bias pin connected to negative supply), the performance of the CA3280 ota will resemble two CA3080-type ota's. When the diodes are biased on, they will effectively reduce the input impedance of the input terminals. This will attenuate the input signal. Thus, due to control of the diode bias current, the input level varies. Also, the signal voltage across the diodes will change in an exponential manner as the input current (through input current-limiting resistors)

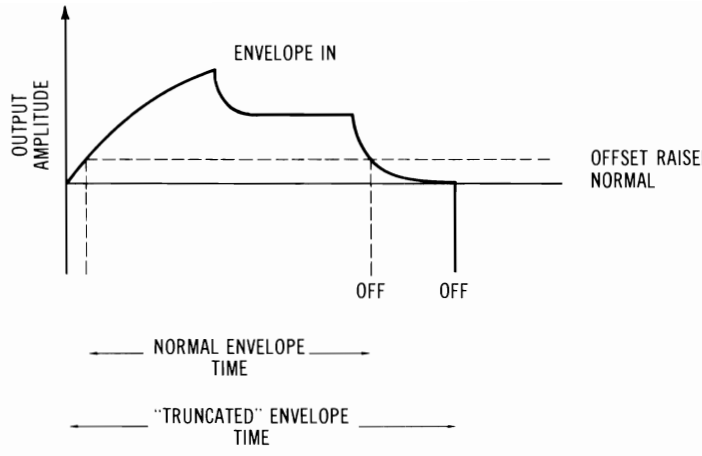



**Fig. 6-7. The effect of offsetting the zero trim of Fig. 6-6.**

changes. This is the now familiar current/voltage characteristic of a semiconductor junction. Since the diodes are internal to the IC, their log characteristics will be almost identical with the input transistors of the (internal) differential amplifier. The two (exponential) distortions cancel, so the input signal level can be higher before distortion occurs. The diodes also have a temperature coefficient that is the opposite of the differential amplifier transistors, so the temperature sensitivity of the circuit is reduced. The value of the input signal current ($I_S$) should always be below the value of the diode bias current ($I_D$) or the diodes will turn off during signal peaks and distortion will occur.

To approximate the magnitude of the signal current, one must first understand the CA3280 input design (as shown in Fig. 6–9). With the input diodes biased on, current will flow through both input resistors ($R_{in1}$, $R_{in2}$) and the diode, which has a resistance $r_d$. A voltage drop will be created across the diodes and is sensed by the differential amplifier transistors and thus the output current gain. If the diode current is increased, the diode resistance decreases and there is less of a voltage drop—thus less output current. If the diodes are biased *off*, the diode resistance is infinite and, since there is no attenuation of the input signal, the differential amplifier is overloaded (distortion). To find the value of the diode resistance ($r_d$) we must first know the diode bias current ($I_D$). This is approximated by

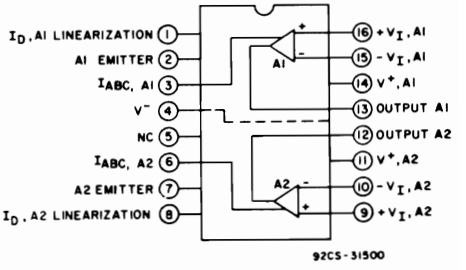
$$I_D = \frac{V_{CC} - V_{EE}}{R_D}$$

where

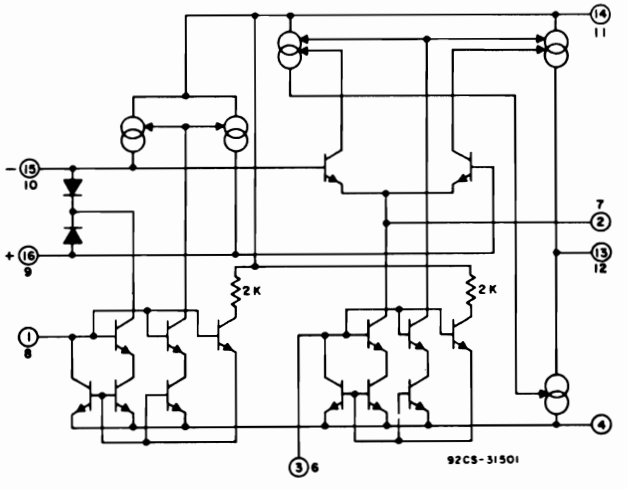
$V_{CC}$ = positive supply voltage,
$V_{EE}$ = negative supply voltage,
$R_D$ = diode bias current-limiting resistor.

Using this diode bias current, we now can determine the diode resistance by the formula (after RCA)

$$r_d = \frac{70}{I_D}$$

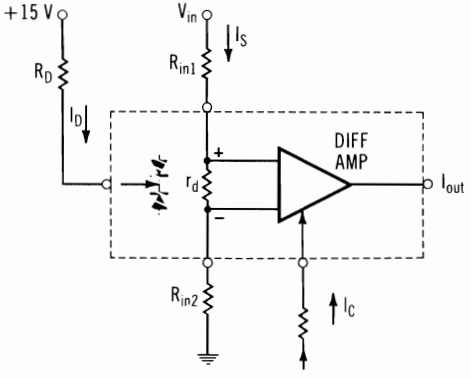



(A) Functional diagram of ½CA3280.

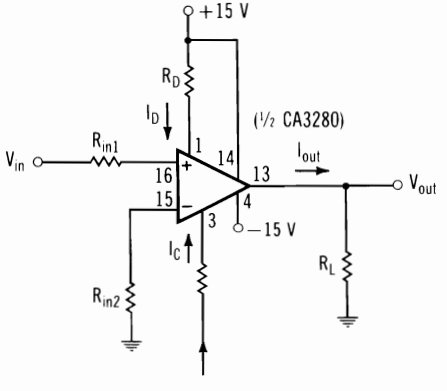



(B) Terminal assignment.

**Fig. 6-8. The CA3280.** *(Courtesy RCA Corp.)*




(A) Input design.




(B) CA3280 connections.

**Fig. 6-9. The CA3280 as a vca.**

where $I_D$ is in milliamperes.

To calculate the gain of the CA3280, we must first know the typical transconductance ($g_m$) with a given control current ($I_C$). The transconductance $g_m$ of a CA3280 is

$$g_m = 16I_C$$

where

$g_m$ is in millisiemens,
$I_C$ is in milliamperes.

If the input diodes are biased *off*, the CA3280 will act like a CA3080 ota, except for the (lower) 16 millisiemens value of $g_m$ as compared to 19.2 for the CA3080. The output gain $A$ in kilohms will then be

$$A = g_m R_L$$

where $R_L$ is the load resistance.

When operating the CA3280 with the input diodes biased *on*, the gain $A$ in kilohms will be

$$A = g_m R_L r_d \, [1/(R_{in1} + R_{in2})]$$

where

$g_m$ is the transconductance in millisiemens,
$R_L$ is the load resistance in kilohms,
$r_d$ is the diode resistance in ohms,
$R_{in1}$, $R_{in2}$ are in ohms.

At this time, information available on the CA3280 is scarce and sometimes erroneous. Little is available regarding performance with different diode bias currents. Lower $I_D$ currents will result in increased distortion. Fig. 6–10 shows a circuit suggested by RCA for 10-V peak-to-peak signals.[4] Note that the vca is set for a gain of 2. It may be necessary to change the load resistor (10 kΩ on pin 16) and/or the control current (on pin 3) to obtain the desired gain.

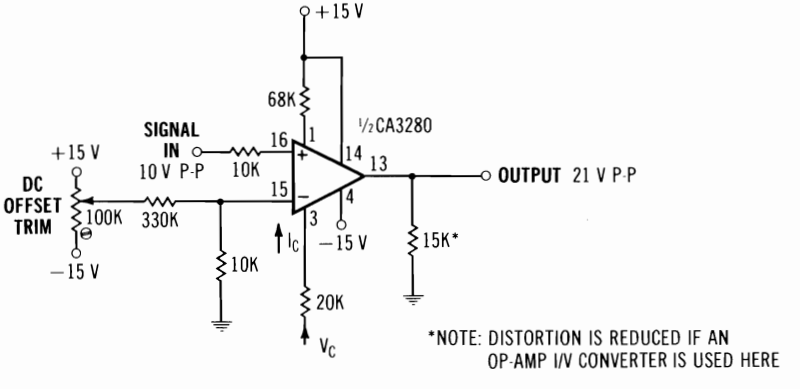



**Fig. 6-10. A CA3280 vca circuit.**

Another feature of the CA3280 is that the differential amplifier emitter connections are brought out on pins 2 and 7. These were used in a triangle-wave-to-sine-wave converter in Chapter 4. These pins could possibly be used as control inputs in conjunction with the $I_C$ pin. All in all, this IC has many possibilities which are just beginning to be explored.

### The LM13600 (XR13600 and NE5517)

These dual ota's are similar in operation to the CA3280. They also contain input linearization diodes, although the method used to internally bias them is different than that of the CA3280 (Fig. 6–11). These ota's do not provide access to the differential amplifier emitters as do the CA3280 ota's, but instead they contain on-chip Darlington transistor buffers. These buffers have an input bias current (impedance) that varies with the ota control current ($I_C$). For high $I_C$ levels, the bias current is higher, resulting in a higher slew rate. The only major disadvantage of these buffers is their −1.4-V offset. If desired, the buffers can be left out of the circuit and replaced with external op amps.

A value of 1 mA for the diode bias current ($I_D$) is recommended by the manufacturers. This is provided by a 15-kΩ resistor connected from pin 2 (or pin 15) to +15 V. The signal current ($I_S$) should be less than half the value of diode bias current:

$$|I_S| < \frac{I_D}{2}$$

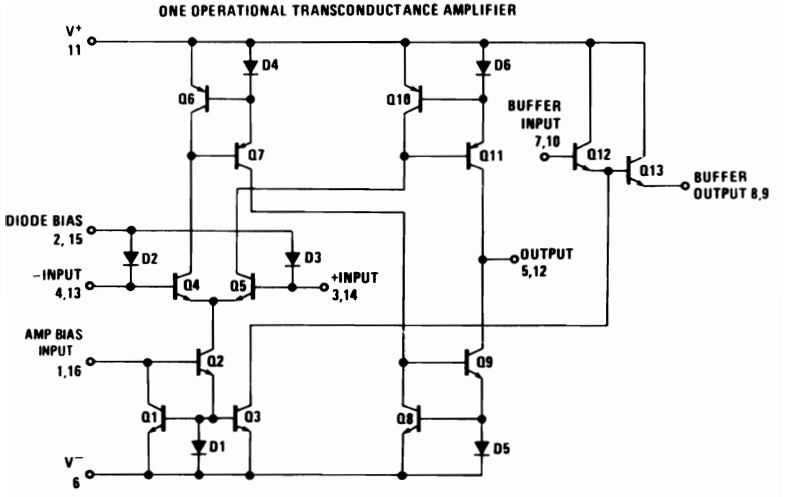
This is because the *diode bias current is split between the two diodes*. If the signal current exceeds the diode current, the diode will be biased off and distortion will occur.

The dynamic resistance $r_d$ in ohms of *each* diode is

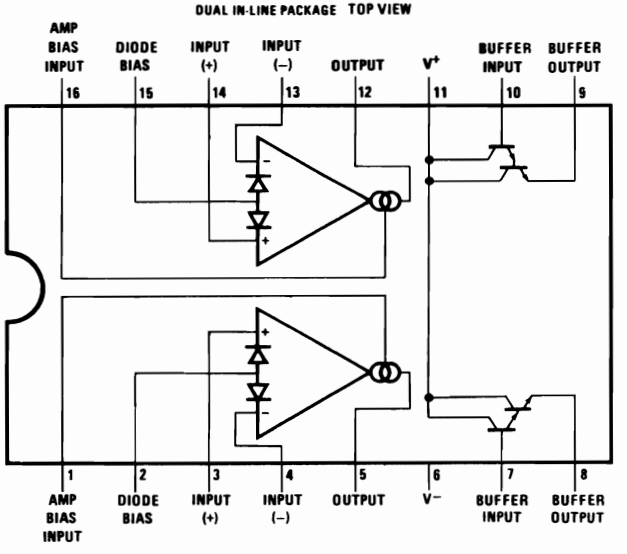
$$\frac{52}{I_D} \text{ or } \frac{104}{I_D} \quad \text{for } \textit{both diodes}$$

where $I_D$ is given in milliamperes. Given this information, you can find the voltage differential across the diode as done previously for the CA3280 (Fig. 6–9). The transconductance in millisemens for the LM13600 is

$$g_m = 19.2\, I_C$$




(A) Schematic diagram.




(B) Connection diagram.

**Fig. 6-11. The LM13600 (XR-13600, NE5517).**
*(Courtesy National Semiconductor Corp.)*

with $I_C$ in milliamperes. Note that this is the same equation as for the CA3080. If the input diodes are biased off (diode pins open), the ota's perform as CA3080-type ota's. The output current of the LM13600 is found by the equation

$$I_{out} \cong I_S \frac{(2I_C)}{I_D}$$

where
$I_S$ is the signal current,
$I_C$ is the control current,
$I_D$ is the diode bias current.

The majority of applications in the application notes from the manufacturers wire the ota inputs as shown in Fig. 6–12.[5] The trimpot is adjusted for minimum control voltage feedthrough. It is suggested that the control current used be as large as possible (but under the 2 mA maximum) to obtain the best signal-to-noise ratio. It is also suggested that the distortion (with fixed diode bias current) be set with $R_{in}$ first, and then the output gain be adjusted by selecting $R_L$.

Although the previous ota designs are very useful and relatively inexpensive, alternate devices are available that offer voltage control of the gain and improved specifications. These devices are used in commercial synthesizers and studio applications.

### The B+B Audio 1538

The B+B Audio 1538 is a dual vca that can be voltage controlled for a range of over 100 dB. It has a signal-to-noise ratio of more than 90 dB and a typical distortion of 0.004 percent! A basic dual vca circuit using the 1538 appears in Fig. 6–13. Op amps IC1 and IC2 buffer the input signals for the input attenuation resistors (R2–R5). This circuit has limited uses as the vca's are not actually separate because of the common control voltage.

The circuit in Fig. 6–14 is an improved performance vca using the 1538. The two internal vca circuits are connected differentially (the signal is inverted through one vca and the two outputs are differentiated). This results in a 3-dB improve-

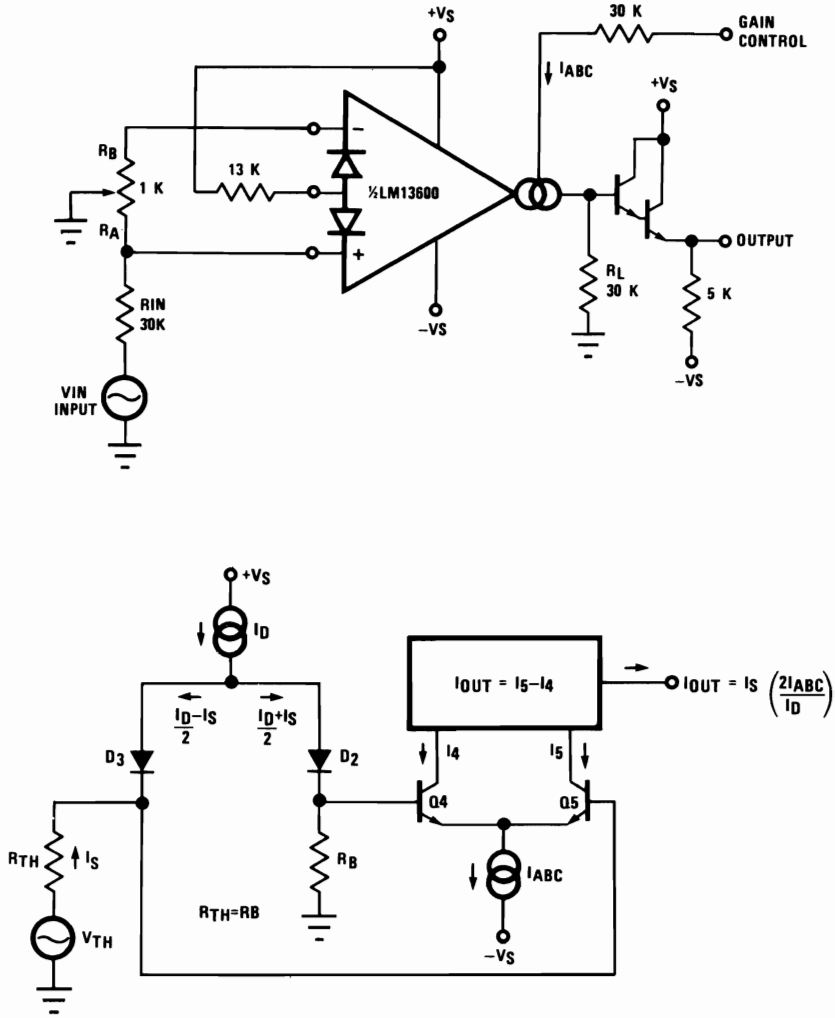



**Fig. 6-12. A vca using the LM13600.**

ment in the signal-to-noise ratio. Trimmer R4 is used to null out any dc shifts that may occur as the control voltage is varied.

Finally, the circuit in Fig. 6–15 is designed for critical, high-performance applications. Op amps IC3 and IC4 act as voltage controlled current sources to improve distortion levels with high-amplitude input signals.

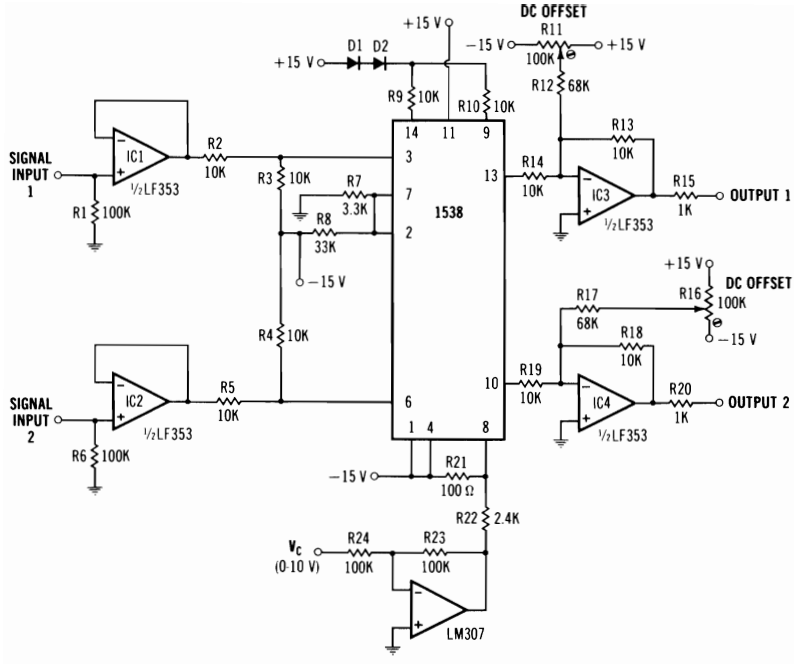



**Fig. 6-13. A dual vca using the B+B Audio 1538.**

## The SSM2020

The SSM2020 is a dual vca designed to be used with external op amps. Simultaneous linear and exponential control of gain is possible using the temperature compensated matched transistors contained in the IC (Fig. 6–16). Each vca has independent control inputs, differential signal inputs, and current outputs. The control range is 100 dB with an 86-dB signal-to-noise ratio and less than 0.1 percent thd.

One half of a dual vca circuit, using the SSM2020 and offering linear or exponential voltage control, is shown in Fig. 6–17. Op amp IC2 and the internal transistors of the SSM2020 work together to form an exponential/linear current sink for the vca. The reference current should be set to one-half of the desired logarithmic control current range. Design formulas are given in Fig. 6–18.

For simple linear control applications the circuit of Fig. 6–19 can be used. Resistor $R_C$ limits the maximum control current.

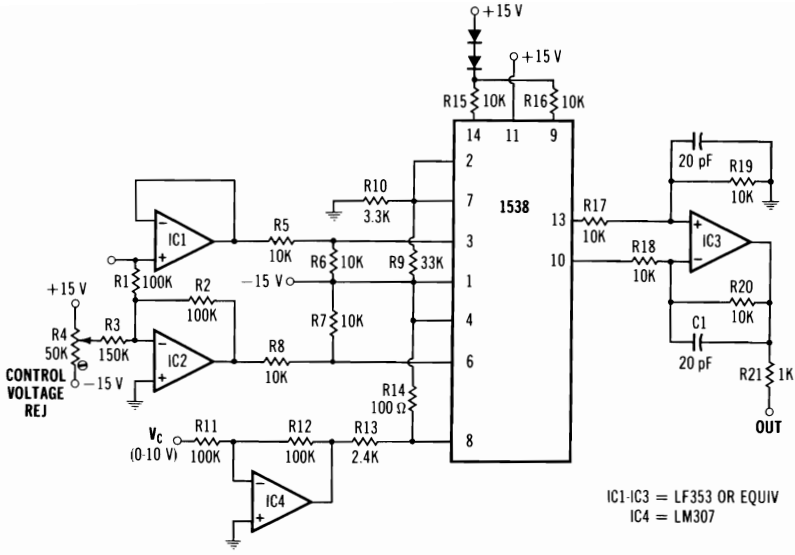



**Fig. 6-14. A general-purpose vca using the 1538.**

Resistor $R_L$ sets the output voltage gain. A control voltage rejection trimmer can be added to the circuit (as in Fig. 6–18) if desired.

As we mentioned in the last chapter, vca's can be used as the control elements in voltage controlled filters (vcf's). Design information for a second-order state-variable filter using a SSM2020 is given in Fig. 6–20. Bi-FET op amps are suggested for use in this circuit. Their low input bias currents will enable the filter to operate over a wide control range. Note that the vca's are functioning as voltage controlled resistors. Their output currents are fed directly into the two op-amp integrators.

## The SSM2022

Another dual vca introduced by Solid State Microtechnology for Music is the SSM2022 (Fig. 6–21). This IC has *internal* control op amps (they were external to the SSM2020 in Figs. 6–17, 6–18, and 6–20). The op-amp summing nodes are brought out as IC pins. The specifications are not as good as those of the SSM2020 (snr of 76 dB and 0.2 percent thd). The SSM2022 was designed for ease of use and polyphonic systems.

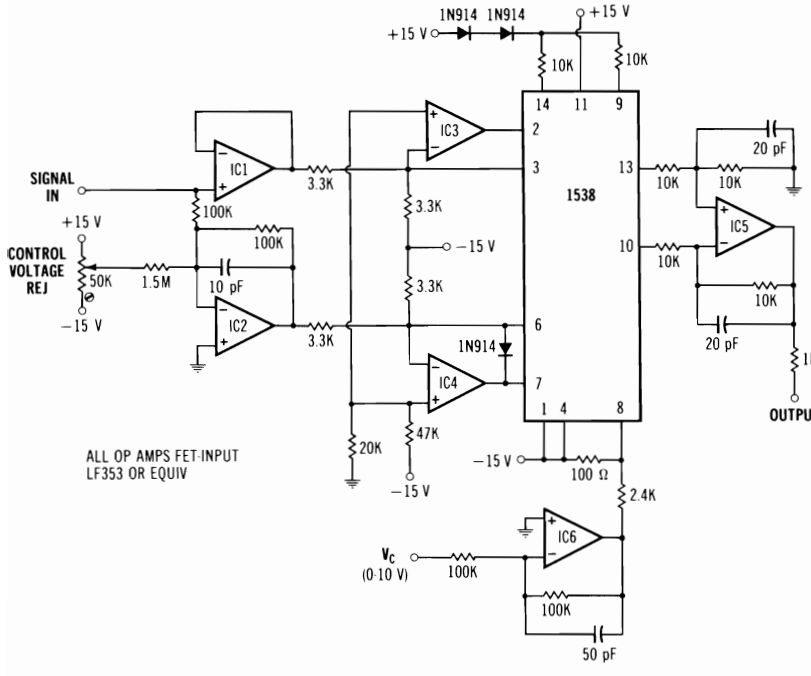
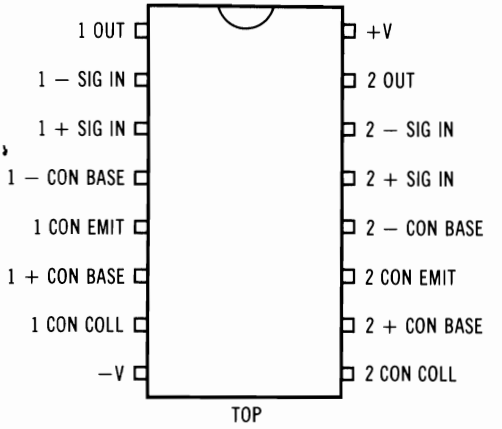


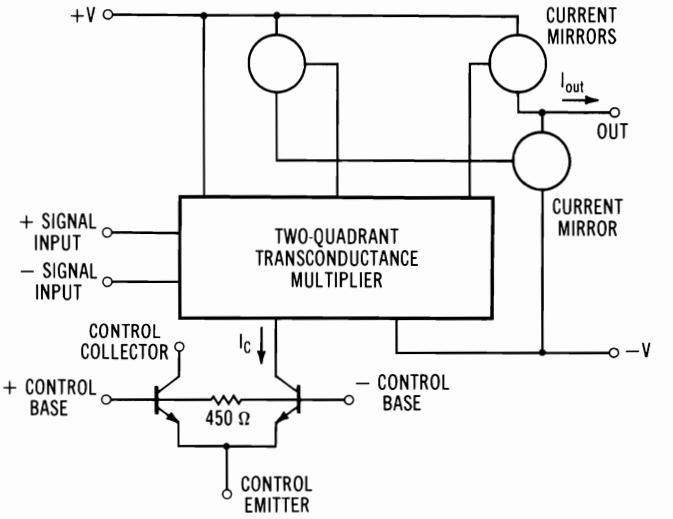

**Fig. 6-15. A high-performance vca using the 1538.**

A basic dual vca using the SSM2022 is shown in Fig. 6–22. The signal inputs (pins 2 and 15) are virtual ground summing nodes. The reference current set at pin 1 by the 24-kΩ resistor determines the level at which the two vca inputs will clip. As shown, the inputs will clip as the sum of the two vca input currents approaches 200 μA. Therefore the input resistors are chosen to limit each vca input to ± 50 percent of the reference current. Assuming a maximum signal input voltage of ± 7.5 V, the input resistor is 75 kΩ for a maximum input current of ± 100 μA. The output current of each vca is converted to a voltage by the familiar op-amp *I/V* converter circuit. A value of 150 kΩ for the op-amp feedback resistor will give unity gain for a control current of 200 μA. The control current is proportional to the product of the linear input current(s) and the negative exponent of the voltage at the exponential control pin. The maximum control current should be within 200 to 400 μA for best performance.

The output current (signal level) increases as the linear con-




(A) Pin diagram.




(B) Equivalent schematic (one side).

**Fig. 6-16. The SSM2020 vca IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

trol voltage becomes more positive. The signal will be completely shut off with a linear control voltage input of 0 V. The linear input pins (pins 6 and 11) are op-amp summing nodes. The 75-kΩ resistors shown correspond to a 200-μA control current for a 15-V input voltage. The exponential control voltage

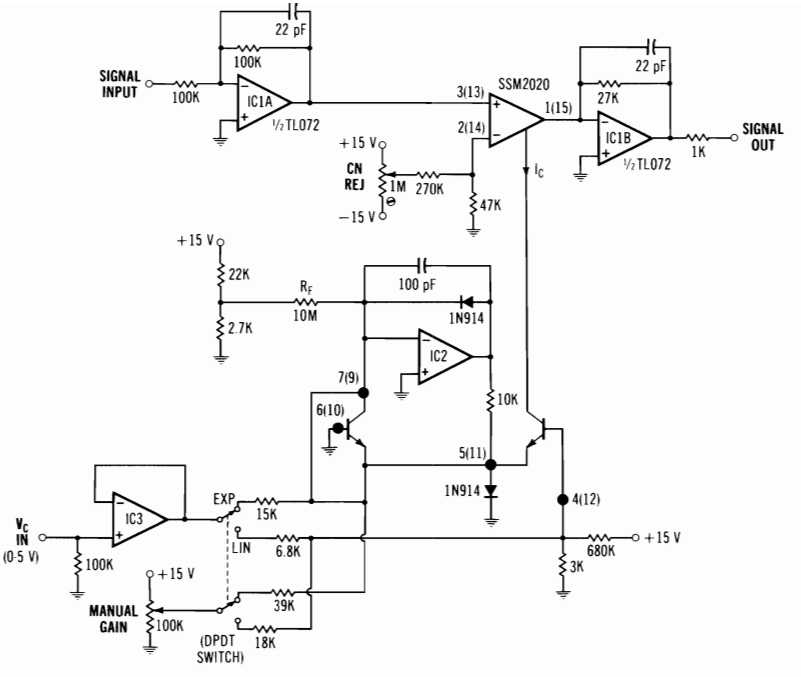



**Fig. 6-17. A vca using the SSM2020.**

inputs operate in an opposite manner to the linear inputs in that a rising input voltage causes the signal to be attenuated more. At 0 volts the circuit gain is unity. As shown, the circuit has a 100-dB control range for a control voltage input of 0 to +10 V.

The 100-pF and 300-pF capacitors provide feedforward compensation for the on-chip control op amp. With these capacitors installed, the circuit bandwidth and slew rate is dictated by the choice of external op amp(s) used in the *I/V* converter.

## The SSM2010

The SSM2010 is a single-vca IC with a signal-to-noise ratio of 90 dB and 0.05 percent thd. It offers linear and/or exponential gain control. It is packaged in an 8-pin minidip package (Fig. 6–23). The above factors and its low external parts count make it a very powerful yet easy to use component. A suggested vca circuit using the SSM2010 appears in Fig. 6–24.

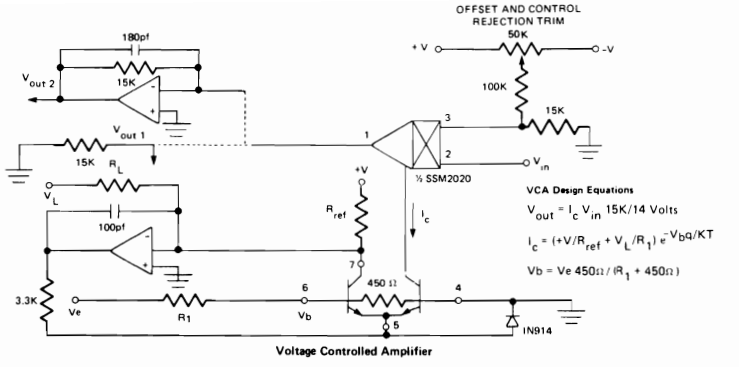



**Fig. 6-18. Design equations for the SSM2020.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

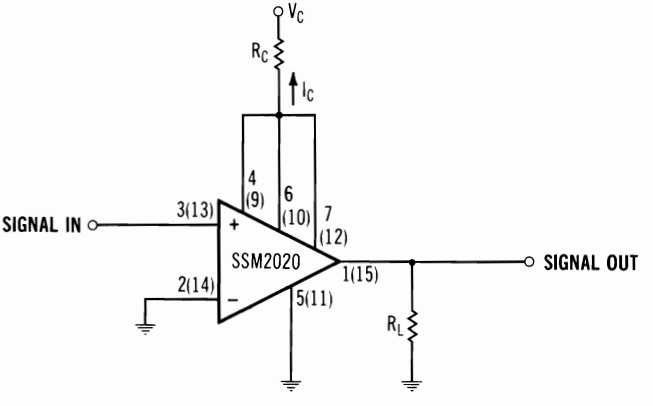



**Fig. 6-19. A simple linear vca using the SSM2020.**

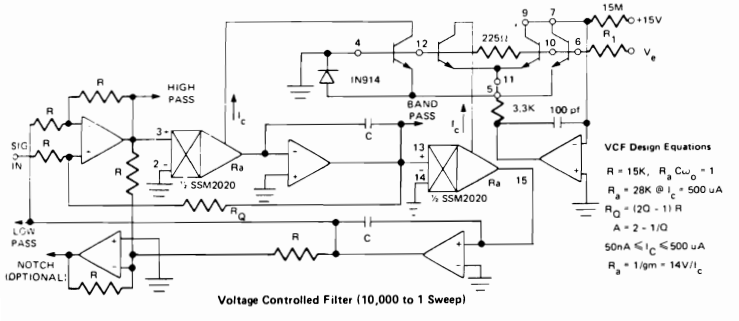
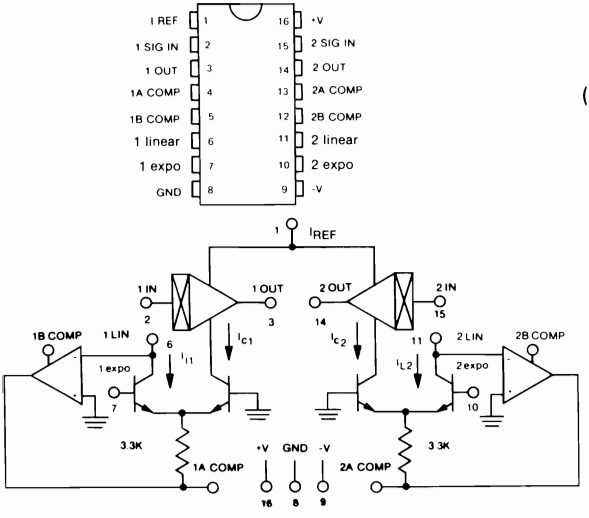



**Fig. 6-20. A state-variable vcf using a SSM2020.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*




(A) Pinout—top view.

(B) Block diagram.

**Fig. 6-21. The SSM2022 vca IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

## The CEM3360

The CEM3360 (Curtis Electromusic Specialties) is a dual vca offering a signal-to-noise ratio of 100 dB, linear or exponential control, and very low control voltage feedthrough (10 mV maximum for 10-V p-p output). The IC is packaged in a 14-pin dual in-line package (Fig. 6–25).

The CEM3360 is designed using a low-voltage IC design technology. The supplies can range up to ± 12 V. The IC may operate at ± 15 V but it is not designed or guaranteed to do so. It is suggested that zener diodes be used to drop the ± 15-V supply levels to ± 12 V.

Note that if the 47-kΩ load resistor is placed in an op-amp *I/V* converter, an inverting op amp at the signal input will be required to keep the same phase relationship, input to output. Also, an attenuator will be necessary to reduce the normal 0 to +10-V control voltages to 0 to +2 V. At a control voltage of 0 V, the input signal will be fully attenuated (0-V input).

## The CEM3330

The Curtis Electromusic Specialties CEM3330 is a dual vca offering linear and/or exponential voltage control of gain. A pin

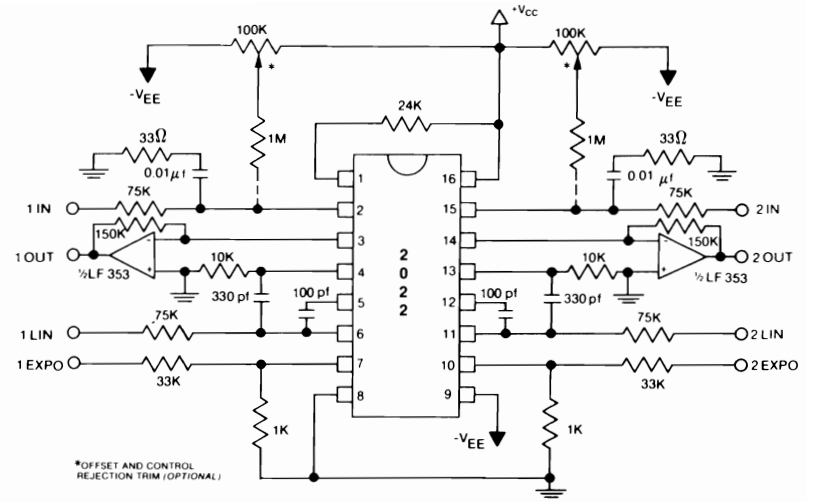
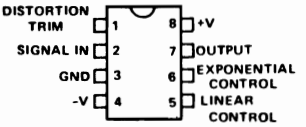
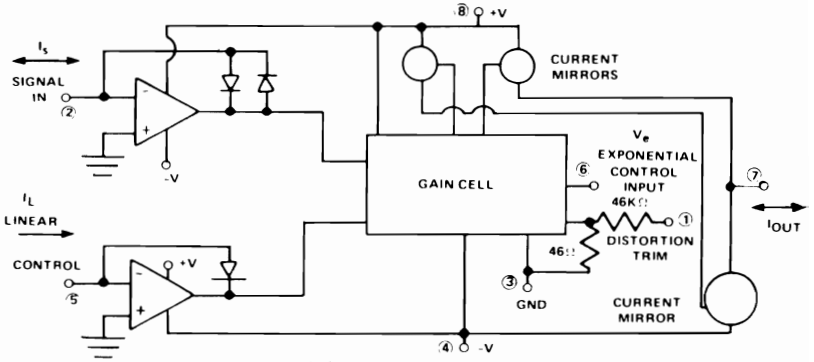



**Fig. 6-22. A dual vca using the SSM2022.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

(A) Pinout—top view.



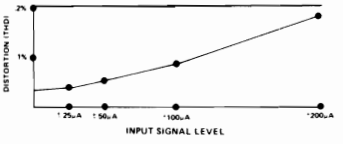




(B) Block diagram.

**Fig. 6-23. The SSM2010 vca IC.**
*(Courtesy Solid State Micro Technology for Music, Inc.)*

diagram of the IC appears in Fig. 6–26. The IC consists of two current-in, current-out gain cells and two log converter circuits. Each log converter generates the logarithm of its linear control

input current (into pins 7 or 12). The exponential inputs have a sensitivity of 18 mV/−6 dB. Thus the more positive the control voltage, the more the output is attenuated. An external inverting




| For best results, select $R_{in}$ to give a ± 50μA input signal current for the maximum average input signal level. | |
|---|---|
| $R_{in}$ | MAXIMUM INPUT SIGNAL LEVEL |
| 50K | ± 2.5V |
| 100K | ± 5.0V |
| 200K | ± 10.0V |

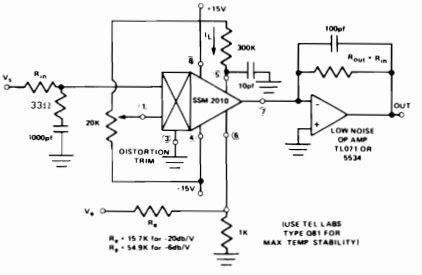
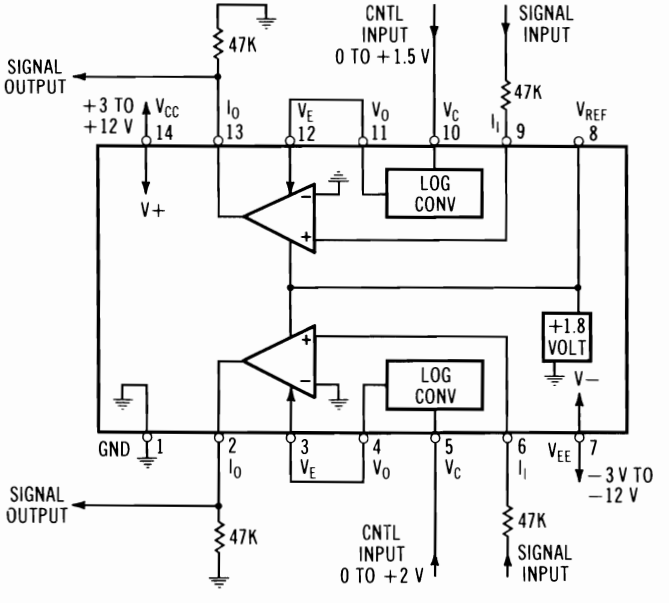



**Fig. 6-24. A vca using the SSM2010.**



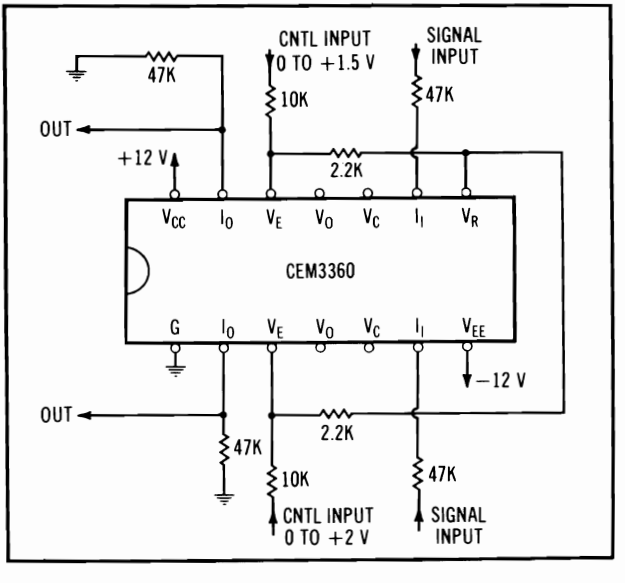

(A) Functional block diagram.

**Fig. 6-25. Connections for the**

op amp is required for the output to increase with an increase in the control voltage. The signal input pin and linear control input pin for each vca are an internal op-amp summing node. This makes external control and signal interfacing easier.

The CEM3330 vca has a control range of 120 dB and a signal-to-noise ratio of more than 100 dB. Distortion is typically less than 0.1 percent. The idle current of the two vca circuits can be set by an external resistor placed from pin 8 to pin 5. Increasing the idle current will decrease distortion, increase the slew rate, and increase the maximum output current at a cost of increased noise and control voltage feedthrough to the output. The vca's should be operated with low idle currents when control of low-frequency signals is desired (less control voltage feedthrough). The effect of idle current on vca parameters can be seen in graphs appearing in the CEM3330/CEM3335 data sheet in Appendix B.

A dual vca circuit using the CEM3330 appears in Fig. 6–27.[6] Op amp IC2B inverts the exponential control input voltage to cause an increase in signal output with an increase in control




(B) Connection for exponential control.

**CEM3360 linear/exponential control vca.**

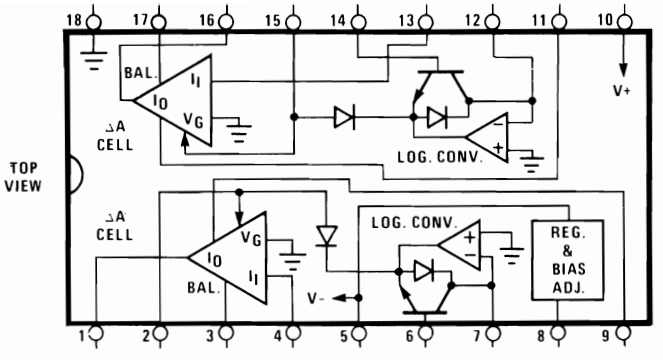



**Fig. 6-26. The Curtis Electromusic Specialties CEM3330 vca IC.**
*(Courtesy Curtis Electromusic Specialties)*

voltage. The switching input jacks shown for this input and the linear control input cause a unity-gain signal output to be generated when no plugs are inserted. This is useful for oscillator tuning or setting up patches. Resistors R25 and R48 (just below the CEM3330) can be switched to both control inputs with a dpst switch (for unity gain), eliminating the need for switching jacks.

The AM input shown for each vca can be used to modulate the linear input control voltage (as tremolo). A 10-V dc signal connected here will cancel out a 10-V linear input control voltage at pin 7 (pin 12) because op amp IC2A is an inverter. The STOP input is meant to cut off the vca output on activation of a foot switch connected to −15 V. A 9-V battery (placed in an external foot switch housing) can be used instead of −15 V if R5 (R29) is changed to 91 kΩ.

The idle current of the vca's is set by resistor R9 (between pins 5 and 8 of the CEM3330). The output current for the CEM3330 is determined by

$$I_{out} = -I_{in} \exp(-V_G/V_T)$$

where

$I_{in}$ = signal input current,
$V_T = KT/q \cong 26$ mV at 25°C, room temperature,
$V_G$ = voltage applied to direct current input pin 2 or pin 15 (from log converter).

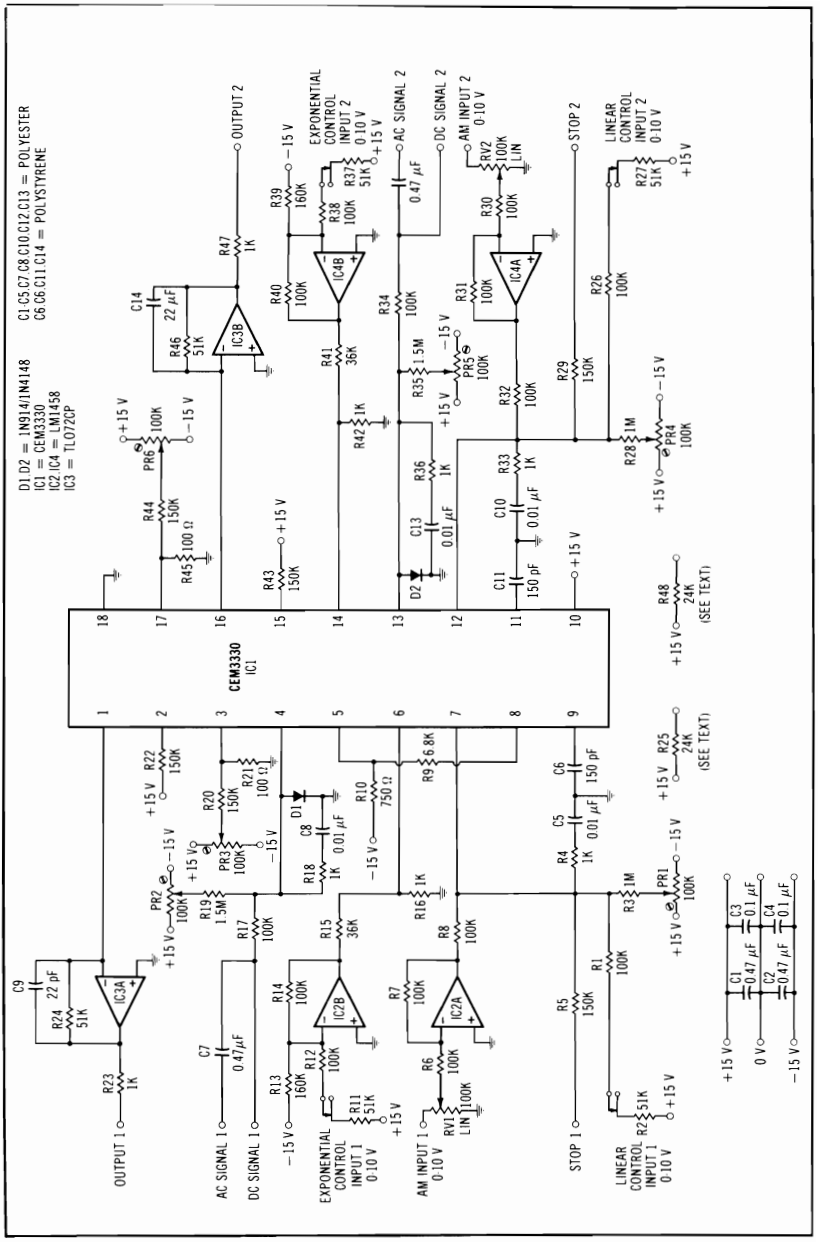



**Fig. 6-27. A vca using the CEM3330.**
*(Courtesy* ETI Magazine *and Digisound, Ltd.)*

The output of the log converter is determined by

$$V_{olc} = -V_T \ln\left(\frac{I_{CL}}{I_{ref}}\right) + V_{CE}$$

where

$I_{ref}$ = current sourced by resistor connected to pin 2 or pin 15, R22 and R43 in Fig. 6–27 (typically 50–150 $\mu$A),

$I_{CL}$ = linear input control current (through input resistors connected to pin 7 (and pin 12),

$V_{CE}$ = exponential control voltage at pin 6 and pin 14.

The output current of the gain cell is given by

$$I_{out} = \frac{-I_{in}\, I_{CL} \exp\left(-V_{CE}/V_T\right)}{I_{ref}}$$

where $I_{in}$ is the signal input current.

To obtain the best signal-to-noise ratio, the signal input current should be as large as possible. However, distortion occurs at levels higher than several hundred microamperes. It is recommended that the signal input resistance (as R17 in Fig. 6–27) be set to limit the input current to within +/− 50 to +/− 150 $\mu$A. A value of 100 k$\Omega$ for $R_{in}$ is typical. The gain of the vca is determined by the control current and the output load resistor, which is usually in the feedback of an op-amp *I/V* converter. The formula for the gain of a CEM3330 is

$$A_V = \frac{V_{out}}{V_{in}} = \frac{R_L}{R_{in}} \times \frac{I_{CL} \exp\left(-V_{CE}/V_T\right)}{I_{ref}}$$

using the preceding formula.

A Tel Labs 1-k$\Omega$ tempco resistor can be used in the attenuator for the exponential control input (in place of R16, Fig. 6–27) to compensate for gain changes with temperature. If linear-only control is used, the exponential input can be grounded and the tempco resistor can be left out.

Control voltage feedthrough is nulled out by trimmer PR2 (PR5). This is adjusted to 0 V at the output with the signal input grounded. Output distortion is minimized by the adjustment of trimmer PR3 (PR6). Connect a fresh 9-V battery (or stable dc supply) between the DC SIGNAL input and ground. Measure the output voltage of the vca. Reverse the dc voltage source connections and measure the vca output voltage again. Trimmer PR3 (PR6) should be adjusted so that the voltages above and below ground are equal.

Trimmer PR1 (PR4) adjusts for precision cancellation of the linear control voltage by the am control voltage. Connect a 0- to 10-V signal to the dc input of the vca. Then apply a 10.0-V dc voltage to the am input. Turn the am level control clockwise (no attenuation) and adjust PR1 (PR4) for a cancellation of the vca signal output.

### The CEM3335

The CEM3335 is a dual vca, similar to the CEM3330, with the exception that the linear control circuitry is omitted. This allows a smaller IC package, as shown in Fig. 6–28.

## FOUR-QUADRANT MULTIPLIERS

Four-quadrant multipliers can be devised in several forms, which we will now examine.

### Using Two OTAs

Fig. 6–29 details a four-quadrant multiplier using two paralleled, linearily controlled, two-quadrant multipliers (see Fig. 6–6).[7] Op amp IC2 inverts the control voltage for the lower vca circuit. Since the control voltage for each vca must be positive (unipolar) for a current out of the ota, only one vca is on at a time. When a control voltage of 0 volts is present (on the Y input) both vca's should be off (no output current). The vca's can be trimmed by only having one CA3080 installed at a time. First, remove both CA3080s and set TP3 for 0 V out of IC6. Then install one CA3080. The input trimmer for the "active" vca is then adjusted for minimum control voltage feedthrough to the output. Once both vca's are trimmed *separately*, both CA3080s can be installed and trimmer TP3 again adjusted for a 0 V output of IC6. Note that the phase relationships of the two

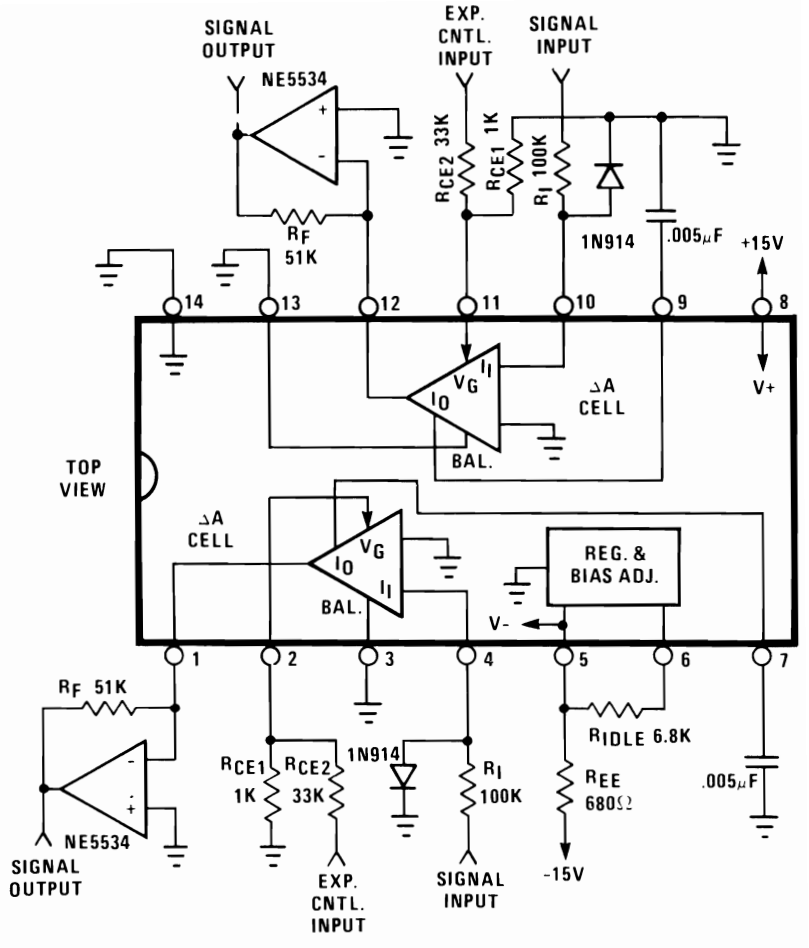



**Fig. 6-28. The CEM3335 vca IC.**
*(Courtesy Curtis Electromusic Specialties)*

CA3080s are opposite each other. This is necessary to achieve the four-quadrant multiplier function. The two output currents of the CA3080s are summed together and converted to a voltage by IC6.

### Using a Single OTA

The circuits in Fig. 6–30 are four-quadrant multipliers that use a single ota. The circuit in Fig. 6–30A uses a CA3080. To trim this circuit, connect a +/− 5-V sine wave signal to $V_Y$ and

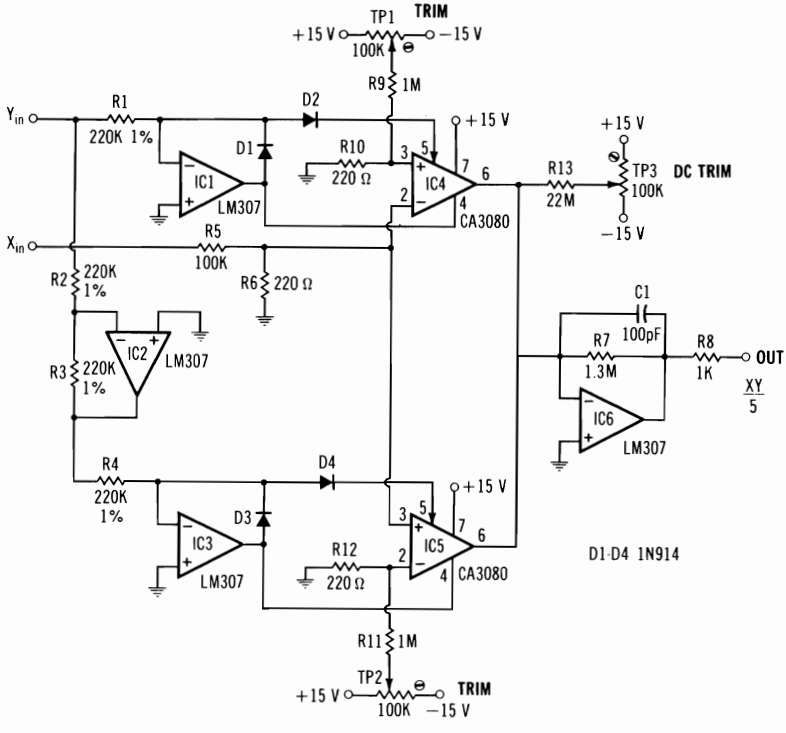
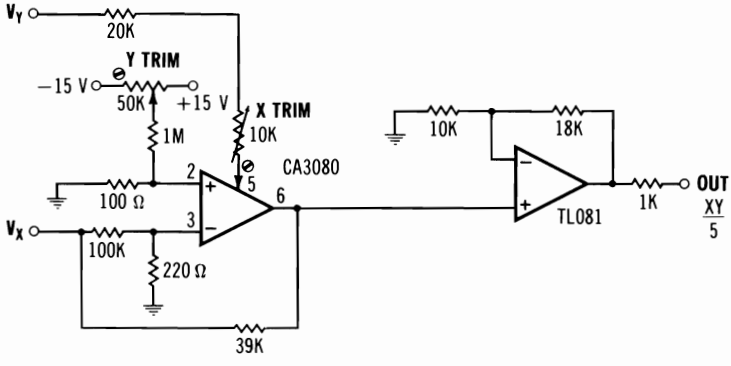



**Fig. 6-29. A balanced modulator using 2 two-quadrant multipliers (vca's),**

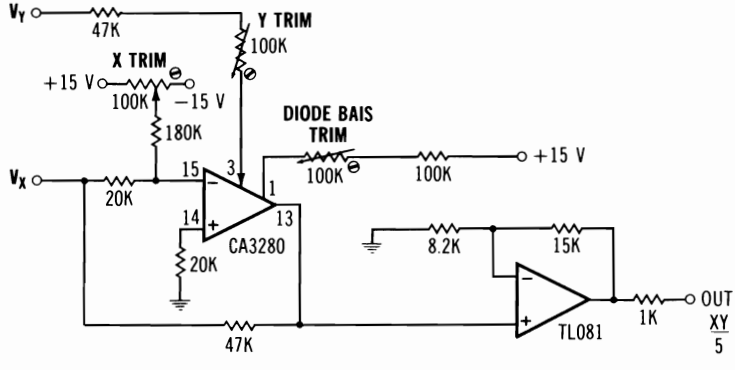
ground $V_X$. Adjust the Y trim for minimum output. Then transfer the signal to the $V_X$ input and ground the $V_Y$ input. Adjust the X trim for minimum output. After the circuit has been trimmed, connect two triangle wave signals (+/− 5 V) to the $V_X$ and $V_Y$ inputs. The output should resemble Fig. 6–31.

Fig. 6–30B illustrates a similar circuit using the CA3280. This circuit contains a trimmer for the diode bias current. This trimmer will interact with both the X and Y trimmers. It is best adjusted by first grounding the $V_X$ input and connecting a +/− 5-V sine wave signal to $V_Y$. Adjust the diode bias trim and X trim for minimum signal output and a dc output level of 0 V. Then switch the ground and signal connections between $V_X$ and $V_Y$ and adjust the Y trim for minimum circuit output. An LM13600 version of this circuit is shown in Fig. 6–30C. Adjustment procedures are similar.

A buffer circuit suggested for the $V_X$ and $V_Y$ inputs is shown in Fig. 6–30D. The buffer presents a low-impedance source to the input resistors in the multiplier. Signals from high-impedance sources would invalidate previous gain and offset adjustments and should be avoided. The $V_Y$ inputs of the previous circuits cannot be directly ac coupled. The buffer in Fig. 6–30D provides ac or dc coupled inputs for $V_X$ and/or $V_Y$. (*Note*: Four-quadrant multipliers can be designed, using this same technique, with any of the current-output vca ICs shown previously in this chapter.)




(A) Using a CA3080.



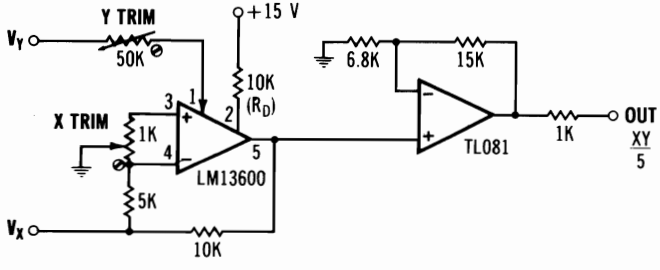

(B) Using a CA3280.

**Fig. 6-30. Four-quadrant**

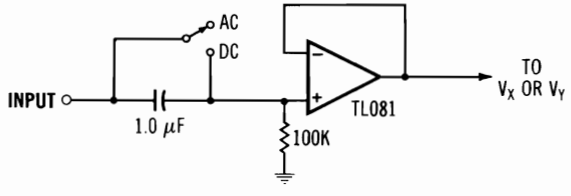
## Multiplier IC Designs

The RC4200 (Raytheon) is an 8-pin multiplier IC that has an excellent nonlinearity specification of ± 0.3 percent maximum. A four-quadrant multiplier can be designed fairly easily with this chip (Fig. 6–32). The offset adjustments ($V_X$ and $V_Y$ null) are carried out using the same procedure as the previous circuits. However, be sure the input level controls are set for maximum input when performing the adjustment procedures. The LF351 op amp provides a low-impedance output. One-percent resistors are suggested for use in this circuit for precise gain matching.

Another multiplier IC that can function as a four-quadrant multiplier is the XR-2228. This IC contains an internal op amp that can serve as an output amplifier for the multiplier section. A four-quadrant multiplier using the XR-2228 is shown in Fig. 6–33. To trim this circuit, first ground both inputs and adjust the output offset for a 0-V output. Then connect a +/− 5-V sine wave to the $V_X$ input and ground the $V_Y$ input. Adjust the Y offset trimmer for minimum output signal. Switch the input connections and adjust the X offset trimmer for minimum output




(C) Using an LM13600.




(D) Buffer for inputs.

**multipliers using one ota.**

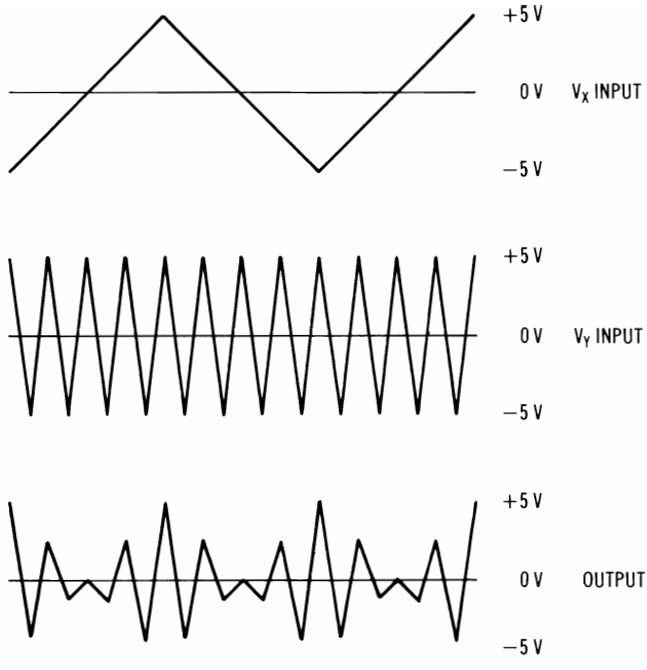



**Fig. 6-31. Signal waveforms of a four-quadrant multiplier.**

signal. Recheck the $V_Y$ adjustment. Finally, connect 5.0 V to both inputs and adjust the gain trim for a −5.0-V output.

Additional four-quadrant multiplier ICs are manufactured by Intech and Analog Devices, among others. Important factors in selecting a multiplier IC are cost and nonlinearity. Nonlinearity is given in percent of full-scale output. Nonlinearities of less than 1 percent are preferred. The cost of a multiplier IC is often a function of its nonlinearity specification. The justification of using a more expensive multiplier IC over a single-ota design will depend on the application. Often, precision is not mandatory and the single-ota design is satisfactory.

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1. Hutchins, Bernie, and Dave Rossum, "Voltage-Controlled Amplifier Design," *Musical Engineering Handbook,* p. 5C (9).
2. Mikulic, Terry, "Reader's Equipment: Four Analog Circuits From Terry Mikulic," *Electronotes,* No. 34, January 1974, p. 16.

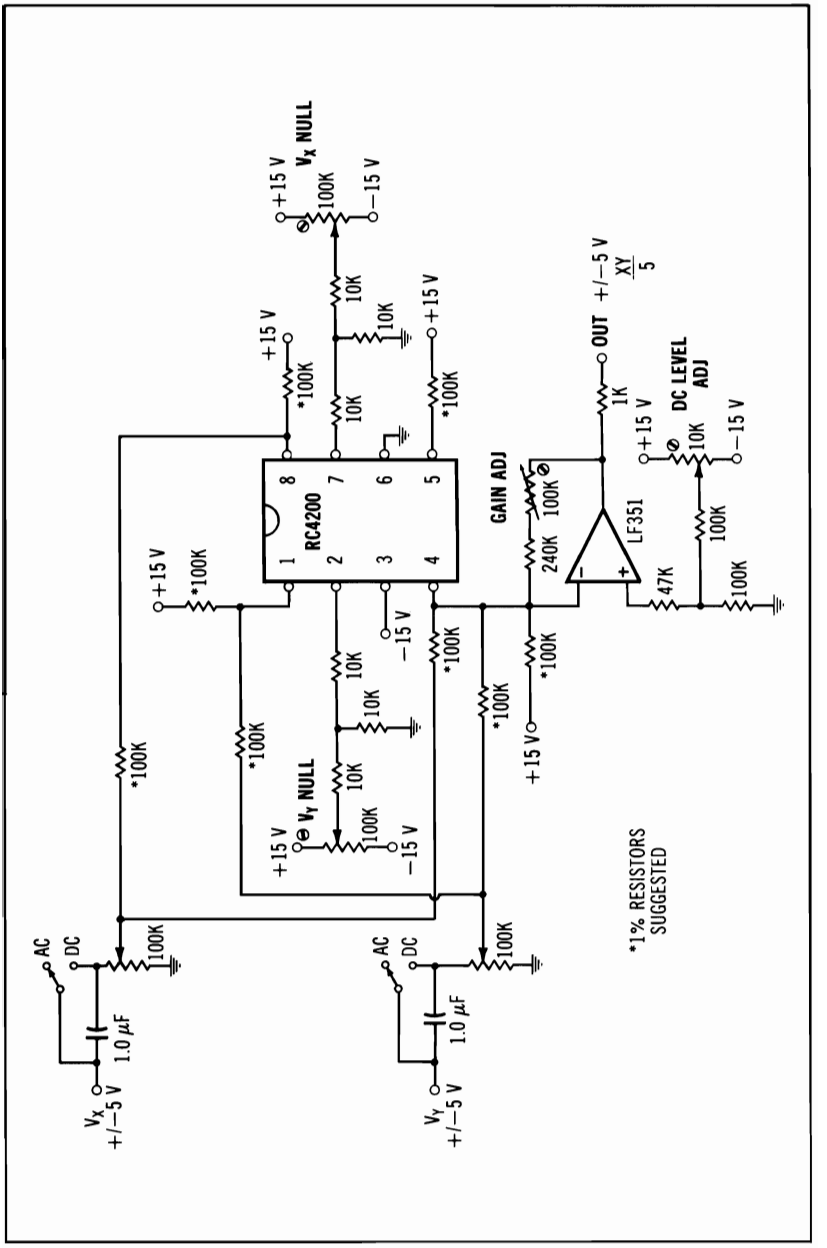



**Fig. 6-32. A four-quadrant multiplier using the Raytheon RC4200.**

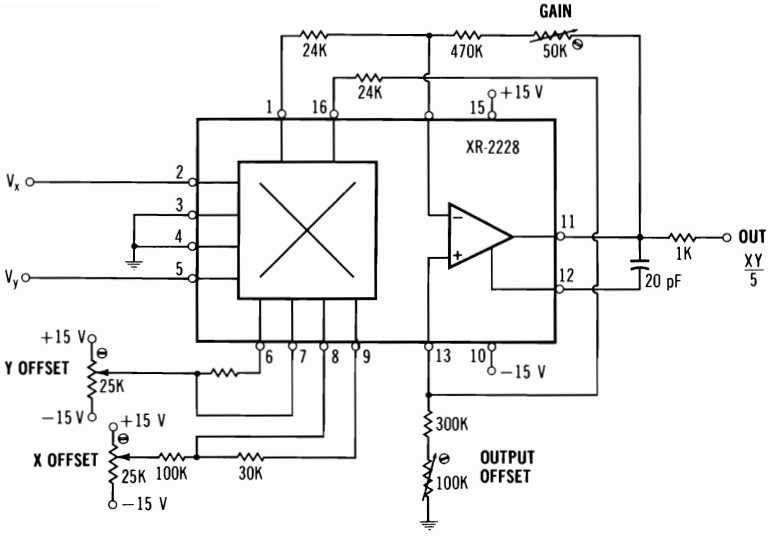
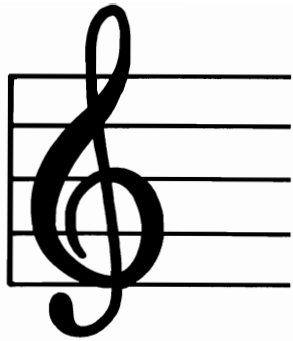



**Fig. 6-33. A four-quadrant multiplier using the Exar XR-2228 multiplier IC.**


3. Hutchins, Bernie, and Walter Jung, "ENS-76 Voltage-Controlled Amplifier— Option 1," *Electronotes,* No. 63, March 1976, pp. 4–6.
4. RCA, *CA3280 Dual OtA, File 1174,* Somerville, NJ 08876, 1979.
5. Exar Integrated Systems, Inc., *XR-13600,* Sunnyvale, CA 94088.
6. *ETI Magazine,* Vol. 9, No. 8, August 1980, pp. 78–81.
7. Hutchins, Bernie, "ENS-76 Balanced Modulation—Option 1," *Electronotes,* No. 63, March 1976, pp. 6–8.

# MISCELLANEOUS CIRCUITS



# CHAPTER 7

In this chapter we will discuss analog delays, mixers, and timbre modulators.

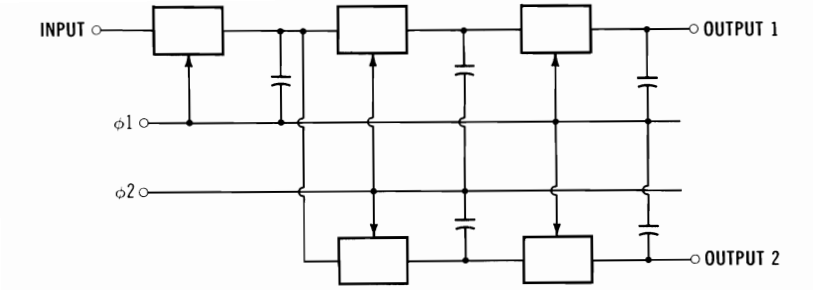
## ANALOG DELAY LINES

Analog delay lines, or "*bucket brigade delay lines*" (bbd's), consist of a series of FET/capacitor sample-and-hold circuits that can be used to delay an audio signal. A two-phase clock (one clock at a logic 1 at the same time the other clock is at a logic 0) is used to alternately switch even and odd sample switches. Thus the analog signal level is loaded into the first stage every time clock phase 1 goes high and, at the same time, charges previously stored in the bbd are transferred to the next adjacent stage. This procedure is detailed in Fig. 7–1. The delay $D$ in seconds caused by the time necessary for the signal level to be passed from the device input to the output is

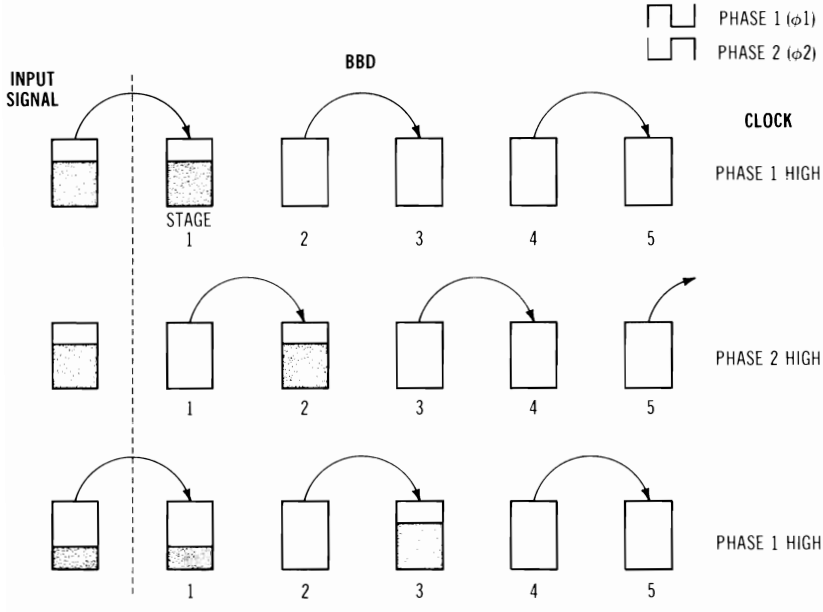
$$D = \frac{N}{2f}$$

where
$N$ is the number of stages,
$f$ is the clock frequency.

The output of a bbd device is made up of *a series of dc voltage steps.* If the clock frequency is low, the input signal must




(A) Circuit.




(B) Movement of charge.

**Fig. 7-1. Charge transfer action of a bbd.**

also be low frequency to obtain a delayed output signal that resembles the input waveform. If the input signal frequency is too high, the bucket brigade will "chop up" the input signal (called *aliasing*), and the output will sound distorted or modulated. To prevent aliasing, the input should be limited (low-pass filtered) to a maximum frequency one-third of the clock

frequency. The output of the delay line will also have to be filtered to remove clock noise from the output and to "smooth" the dc voltage steps. The noise is due to high harmonics created by the steps in the output waveform.

Delay lines are inherently quite noisy and accept relatively small input signal levels. When the input to the delay line is overloaded, severe distortion occurs. Given this information, there are two ways to use bucket brigade delay lines. One is to use a low-level signal with the device, making sure that the signal peaks do not overload the input of the device. This results in a low signal-to-noise ratio. Another method is to run a constant (or nearly so) maximum level (before distortion) through the device. For the majority of uses in a synthesizer, we will be using constant level signals (± 5 V) with the delay module. All we must do is attenuate the signal going into the bbd, and amplify it when it comes out.

If you wish to run a *varying amplitude signal* (such as the signal from a guitar) into a delay line and wish to conquer the noise problem, the solution is to use a *compander.* One section of a compander, called the *compressor,* attenuates the input signal as it rises in amplitude. The higher the input signal tries to go, the more the compressor tries to cut it down. This signal is then fed into the bucket brigade device. The output of the bucket brigade device is fed into the second half of the compander, called the *expander.* This portion does the exact opposite job of the compressor. It will have higher gain for lower input level signals. Thus it boosts the output of the bucket brigade back up to the original signal level. Several compander circuits are available, such as the Signetics NE570/571 (Fig. 7–2). These work well for most applications. Companders can also be made discretely with vca's and envelope followers (Fig. 7–3).

## COMMON EFFECTS USING BBD'S

If the frequency of the clock to the bbd is varied, the delay time of the device will also vary. If the clock frequency is modulated with a periodic signal (Fig. 7–4A), vibrato can be achieved. The frequency of the input signal will be shifted to a higher frequency as the clock frequency is constantly increased. It will be shifted to a lower frequency if the clock frequency is

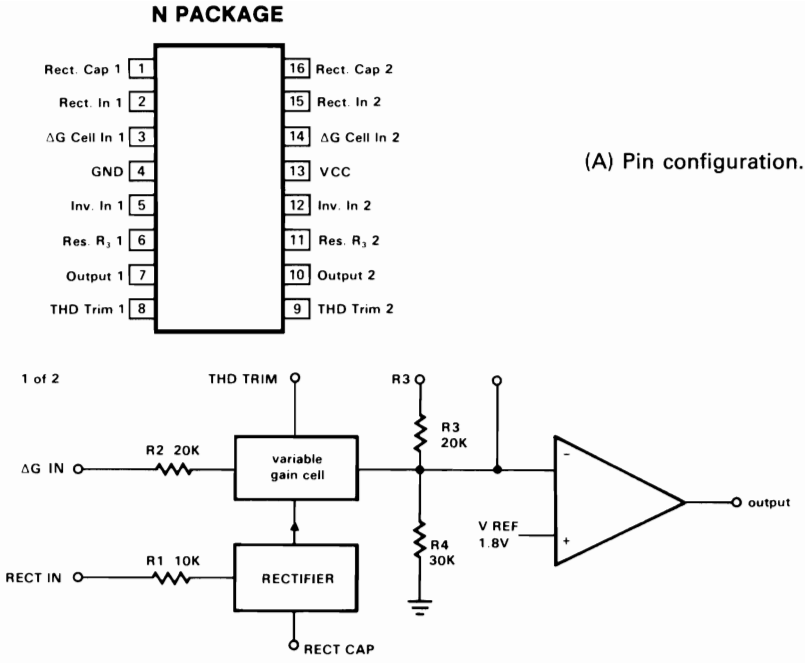


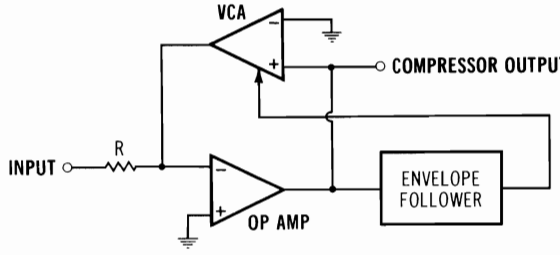

**Fig. 7-2. The NE570/571 compander IC.** *(Courtesy Signetics Corp.)*

constantly decreased. To make a frequency shifter, all that is needed is to voltage control (vc) the clock frequency with a ramp waveform (sawtooth). This is shown in Fig. 7–4B. However, noticeable glitches will occur along with changes in the noise level each time the range is repeated.

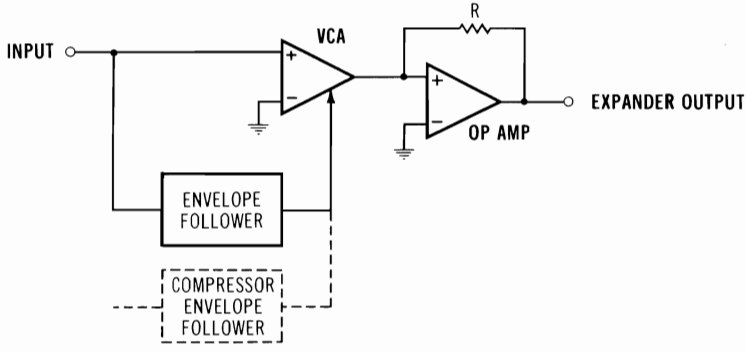
If the output of the bbd is fed back (in phase) into the input of the bbd device, mixing with the input will occur, and an effect termed *flanging* is achieved (Fig. 7–4C). Numerous sharp peaks are created in the output frequency spectrum. The sound becomes increasingly hollow or tubular as the feedback or regeneration is increased.

Summing the input and output of the bbd together results in a similar effect called *chorus* (Fig. 7–4D). This is a smoother, more natural sounding effect that is very pleasing with input signals rich in harmonics. More notches are created in the output frequency spectrum as the clock frequency is increased.

An *echo* effect is achieved by mixing a fixed delay signal with




(A) With input resistor.




(B) With feedback resistor.

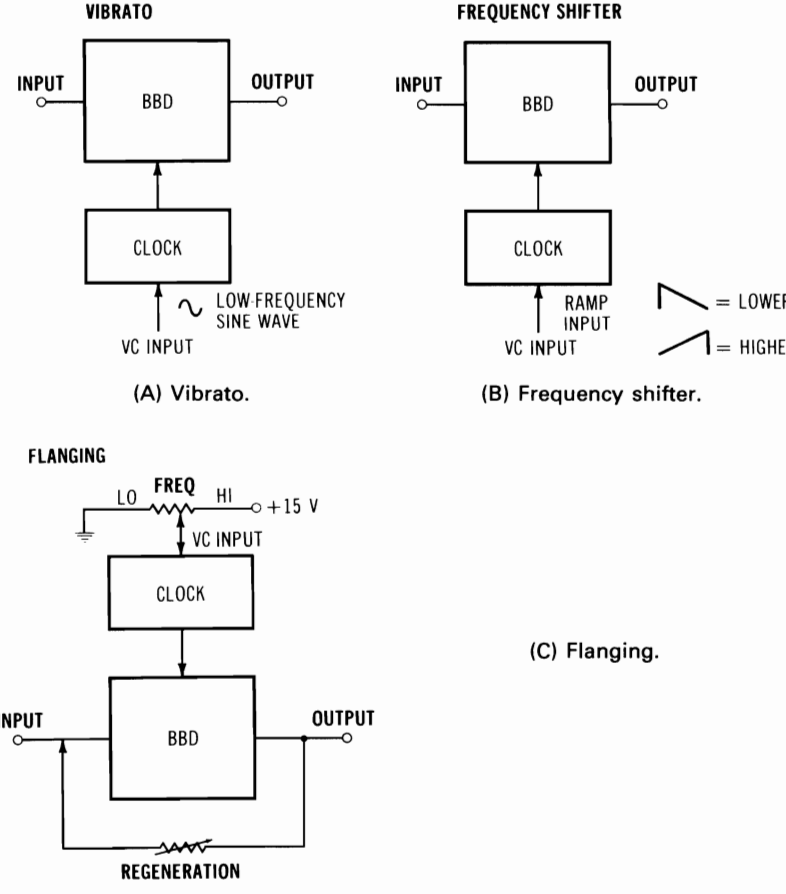
**Fig. 7-3. A compander using vca's and envelope followers.**

the input signal (Fig. 7–4E). To create enough delay to be noticeable, either a low clock frequency (possible aliasing and noise problems) or a device (or series of devices) with many stages must be used. As the regeneration is increased, the number of echo repeats will increase until finally the circuit will saturate.

The number of bbd devices available has increased dramatically in the past few years. This is due to the widespread use of bbd's in flangers, echo devices, artificial reverbs, stereo simulators, etc. A similar device, the *charge-coupled device* (CCD), is another type of analog delay line that can be used in the same manner. Instead of actual capacitors formed on the integrated circuit die, minute charges built up on MOSFET gate channels are used. The gates are biased above the MOS threshold and charges are passed serially as with the bbd de-

vice. Manufacturers of bbd and/or CCD devices include Reticon, Panasonic, Signetics (Philips), and Fairchild. Devices are available with less than 256 stages up to 4096 stages or more. Devices with at least 512 stages can be used for vibrato, chorus, and flanging effects. Echo usually requires devices with more stages.

A simple circuit for a voltage controlled clock is given in Fig. 7–5A. Here, a voltage controlled oscillator is formed with a 4007 CMOS building block. It consists of two inverters and one transistor functioning as a voltage controlled resistor. The output of the oscillator is fed into a 4013 CMOS flip-flop which




(A) Vibrato.

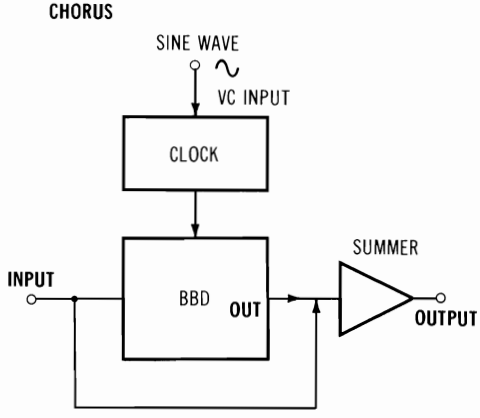
(B) Frequency shifter.

(C) Flanging.

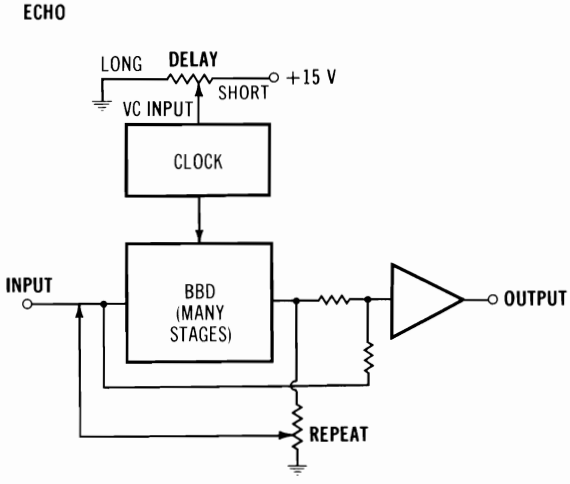
**Fig. 7-4. Various sound effects**

divides the input frequency by 2 and generates two out-of-phase clocks. The output frequency can range from 20 kHz to 60 kHz with a 0 to +15 V control voltage. A low-frequency oscillator that can be interfaced with the vc clock for automatic sweep is shown in Fig. 7–5B.

Sample bbd circuits are shown in Fig. 7–6. As can be seen, the devices are easy to work with. All require trimming the dc

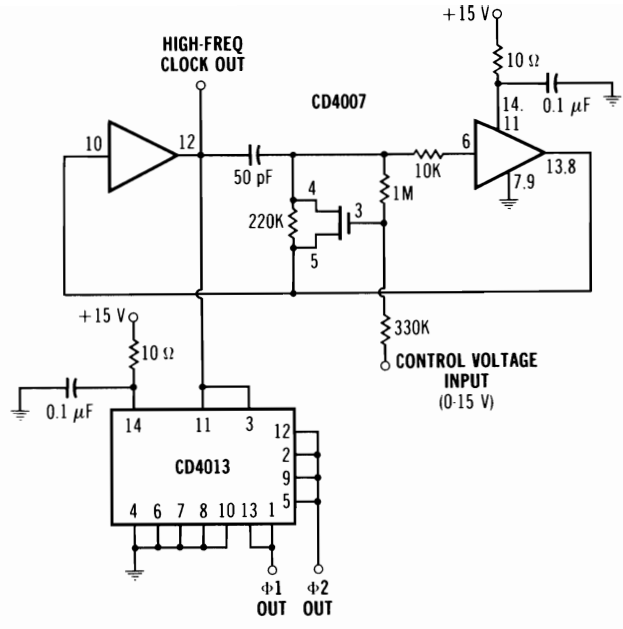



(D) Chorus.

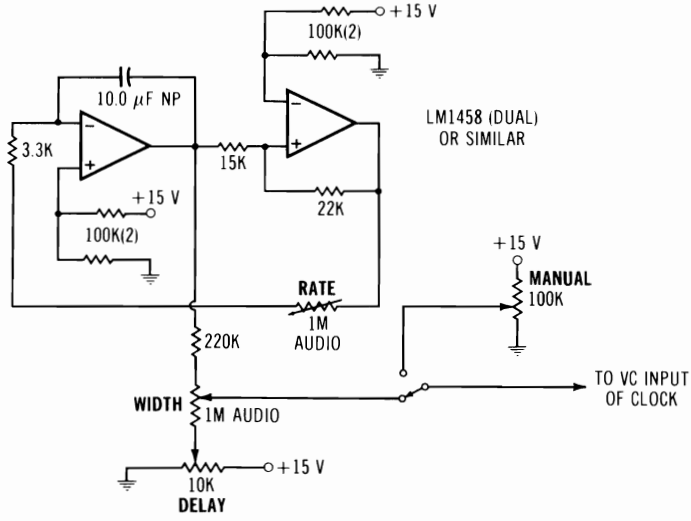



(E) Echo.

**obtained from using bbd's.**

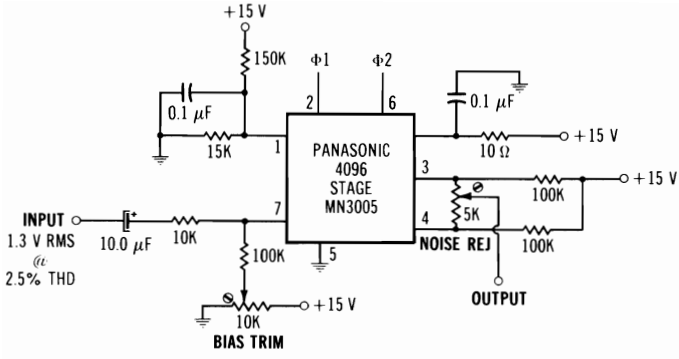



(A) A voltage controlled clock for bbd's.

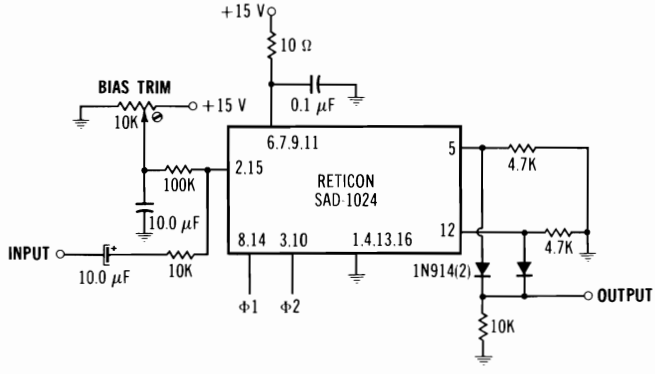



(B) A low-frequency oscillator for use with a voltage controlled clock.

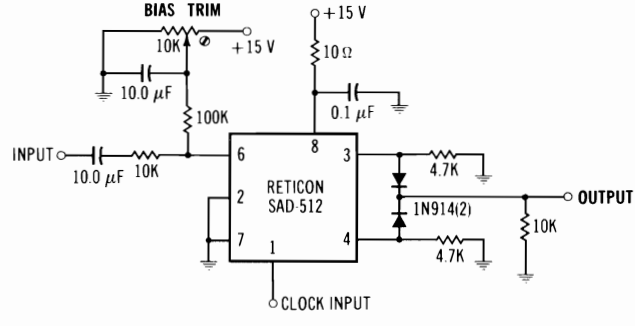
**Fig. 7-5. Clock circuitry for bbd's.**




(A) Using an MN3005.




(B) Using an SAD-1024.




(C) Using an SAD-512.

**Fig. 7-6. Some bbd circuits.**

level of the input signal (bias) for minimum distortion. This is accomplished by observing the device output on an oscilloscope and, with a maximum level input signal input, adjusting the trimmer for minimum distortion on both the positive and negative signal peaks. Some circuits also contain a clock noise trimmer that cancels clock transitions imposed on the output signal.

When laying out a printed circuit board for a delay circuit, be sure to keep traces short. The clock inputs of most bbd ICs have relatively high input capacitances. This will reduce the amplitude of high-frequency clock signals if the traces are long and/or the output impedance of the clock is high. Keep the clock circuitry separated from the audio portions of the circuit to prevent superimposing clock noise on audio lines. Some manufacturers recommend double-sided pc boards for bbd circuits. One side is used as a ground plane (all ground connections are common to this side). This is said to result in a higher signal-to-noise ratio.

## MIXER CIRCUITS

A mixer can be used to sum signals or control voltages. The output may be used as a control voltage or as a final audio signal to drive an output amplifier. A simple four-channel mixer appears in Fig. 7–7. The inputs can be ac or dc coupled. The signal phase can be inverted by connecting it to IC1B. Op amp IC1A inverts signals to get an in-phase signal at the mixer output. An offset control can be added as shown if you wish to shift the output dc level for possible control voltage uses.

## TIMBRE MODULATORS

A *timbre modulator* alters the timbre of an input signal by direct manipulation of the signal waveform. This manipulation can take the form of nonlinear distortion, full-wave rectification, and variable-level clipping circuits. Timbre modulation lets us generate drastic timbre changes with fairly simple circuitry. One such timbre modulator is shown in Fig. 7–8.[1] It consists of a CA3080 vca with an op-amp current-to-voltage converter, a zener diode network, and an op-amp summing amplifier. A control voltage into the ENV IN input is used to linearly control the

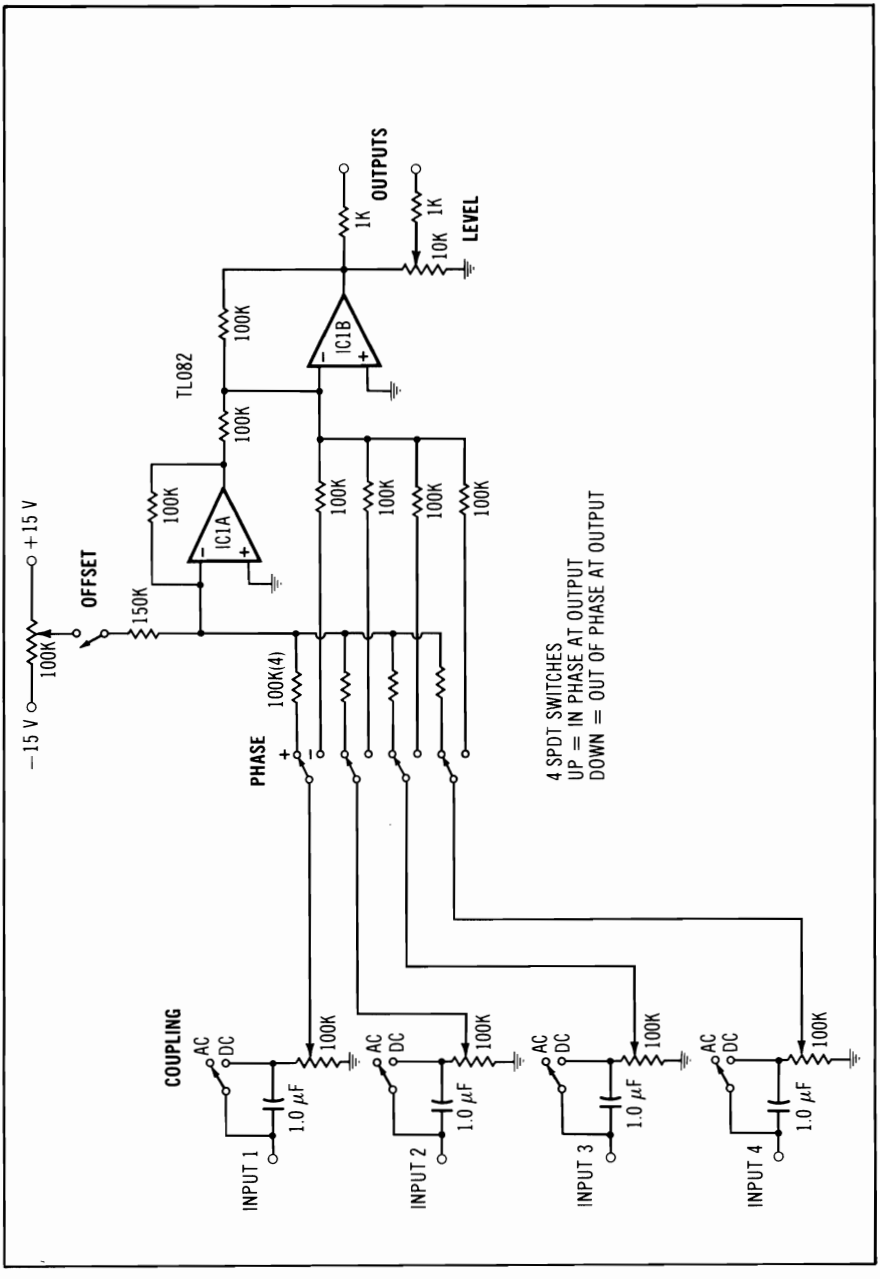



**Fig. 7-7. A four-channel mixer.**

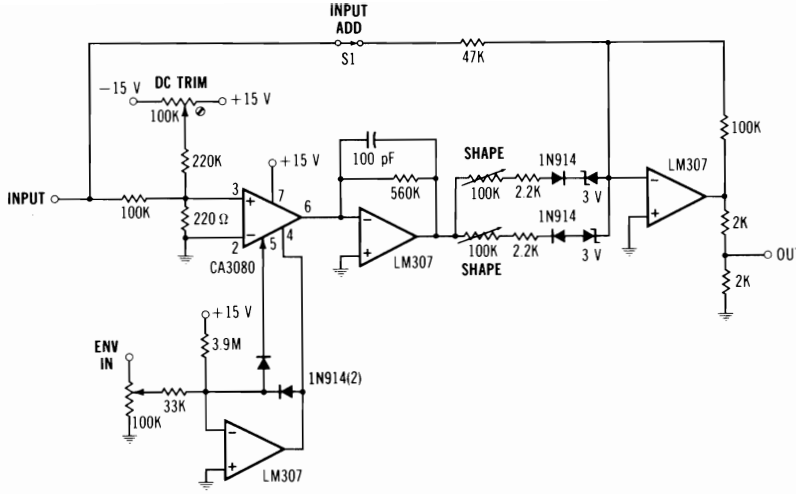



**Fig. 7-8. A timbre modulator.**

gain of the CA3080 vca. The output of the vca is converted to a voltage, which is then fed into two back-to-back zener diode networks that pass the signal only when its amplitude is greater than the zener voltage. The two SHAPE controls vary the amplitude of signal through the zener diodes and thus the gain of the summing amplifier. Typical waveforms generated by this circuit are shown in Fig. 7–9. The most useful effects are obtained when switch S1 is closed.

The output of the timbre modulator given in Fig. 7–10 varies from a full-wave rectified version of the input signal to a square wave (at the signal frequency).[2] This circuit consists of a full-wave rectifier (IC1 to IC3), a ground-referenced comparator (IC5), and two vca circuits (IC6 and IC7 along with IC9 and IC12). The two vca's are used with opposite-polarity control signals. This causes one to increase in gain while the other decreases in gain. When the two ota outputs are summed (into IC11), panning from the sine wave to a rectified sine wave is achieved as the control signal is varied. Typical waveforms generated by this circuit are given in Fig. 7–11.

The timbre modulator in Fig. 7–12 consists of two banks of four lfo/comparator sections. The input signal is compared to the oscillator output for each of the four lfo/comparator sections.

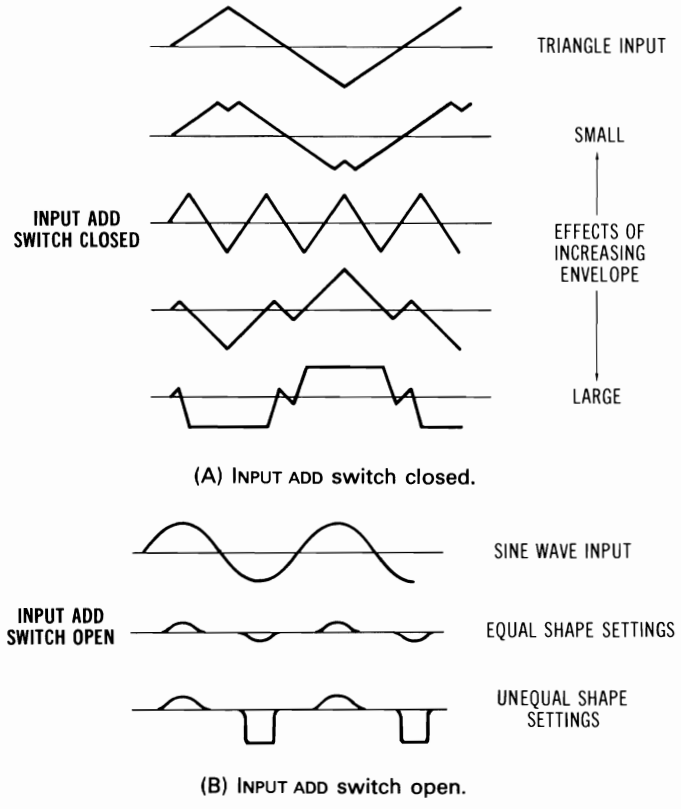



**Fig. 7-9. Waveforms of timbre modulator of Fig. 7-8.**

The comparator outputs are then summed together for the final bank output. The original signal can also be summed in with the closing of the MIX switch, S1. An identical bank of lfo/ comparators will accept the same input (if no input is connected to input 2) due to the switching jack used. The BOTH output will be either an inverted version of the bank 1 output (with 50 percent gain) or a sum of the two bank outputs, depending on the setting of the OUTPUT MIX switch, S2. Fig. 7–13 shows typical (instantaneous) single-bank signal outputs for a triangle wave input. This circuit is used to increase the harmonic content of an input signal. The sound of the output is "fatter" than the input. This module can be placed in front of a vcf to produce more natural sounding timbres.

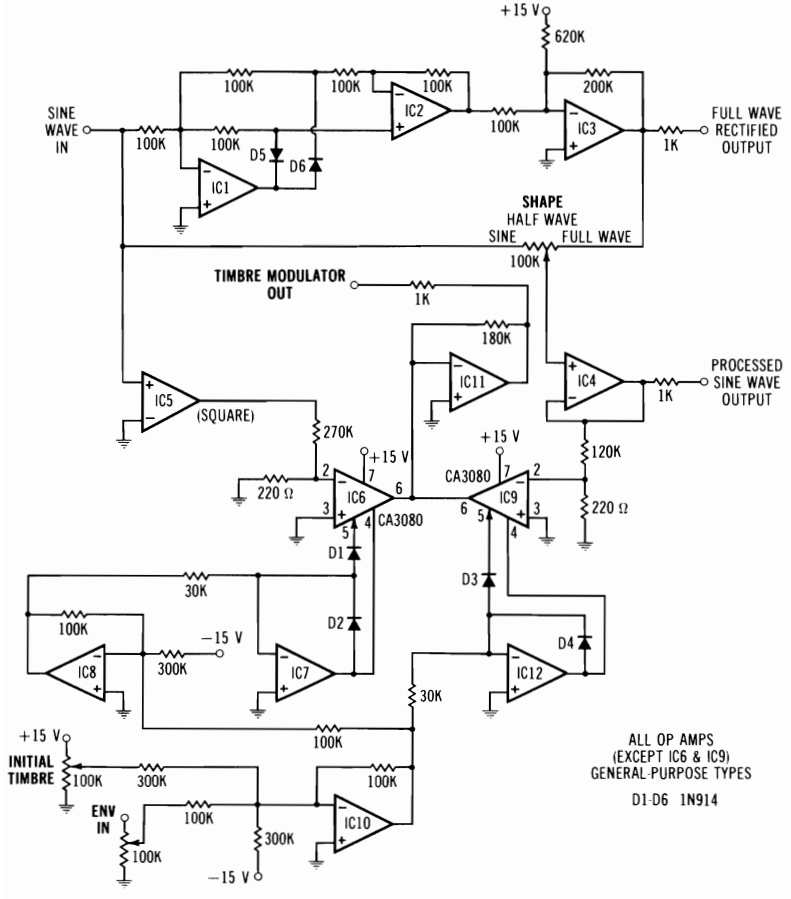
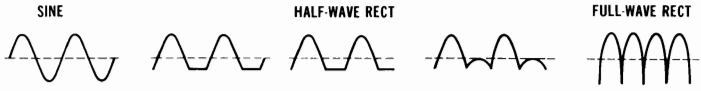



**Fig. 7-10. A sine-wave timbre modulator.**

## REFERENCES

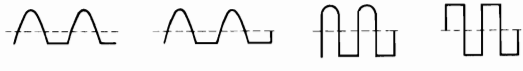

1. Hutchins, Bernie, "Timbre Modulation—Option 1," *Electronotes,* No. 72, December 1976, pp. 24–16.
2. Hutchins, Bernie, "An Odd-Harmonic to Even-Harmonic Timbre Modulator," *Electronotes,* No. 84, December 1977, pp. 9–13.




(A) Output of IC4 as SHAPE control is varied.

(B) Output of IC11 as control input voltage is varied (SHAPE set at SINE).

(C) Same as (B) with SHAPE at FULL WAVE rectified.



(D) Same as (B) with SHAPE at HALF WAVE rectified.

**Fig. 7-11. Waveforms generated by the circuit of Fig. 7-10.**

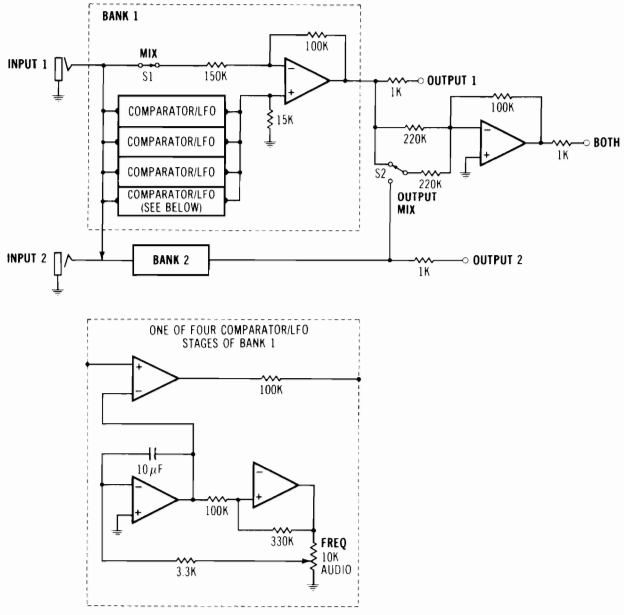



**Fig. 7-12. A timbre modulator using signal comparators and multiple lfo's.**

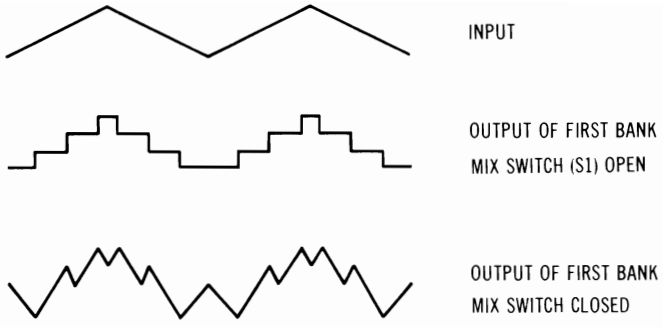
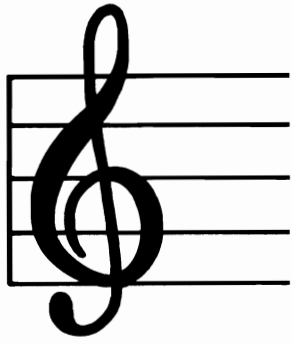



**Fig. 7-13. Typical waveforms generated by the circuit of Fig. 7-12.**

# THE MODULAR SYSTEM



# CHAPTER 8

The intrigue of building a modular synthesizer is that you never have to stop. You soon acquire an insatiable desire to make your system larger. Most of us will never complete our dream system due to time and/or money limitations. Smaller systems will provide a lot of enjoyment, and, with use, will increase your knowledge of music and electronics. It is best to start out small, learning all you can about the basic synthesizer modules, before attempting to make the system more complex.

## THE BASIC SYSTEM

A basic synthesizer will consist of the following:

1. A keyboard interface (and keyboard).
2. A vco.
3. A vcf (usually low-pass).
4. An envelope generator.
5. A vca.

Such a system is illustrated in Fig. 8–1. This is the basic monophonic synthesizer "voice." Sound is produced by the vco at a frequency determined by the keyboard control voltage. An envelope generator, triggered by the keyboard, controls the cutoff of the vcf and thus changes the timbre of the sound. This same envelope generator controls the amplitude of the sound through a vca.

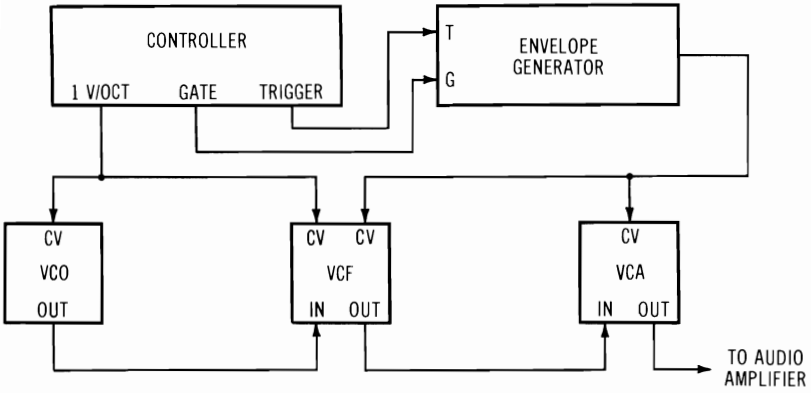



**Fig. 8-1. A basic monophonic synthesizer.**

The first module that you will want to build will probably be the vco. It is always satisfying to build something that you can listen to right away. You can vary the frequency with a front-panel FREQUENCY control and listen to the differences in sound between the various output signals. You will, however, have to attenuate the +/− 5-V signal generated by the vco with a potentiometer to prevent overloading (clipping) the input of your audio amplifier (see Fig. 8–2).

The next module that you will want to build is the vcf. Most general-purpose vcf's are 2- or 4-pole, low-pass filters. With a vcf you can change the timbre of the vco sound with the vcf cutoff frequency control (Fig. 8–3). You can also listen to the

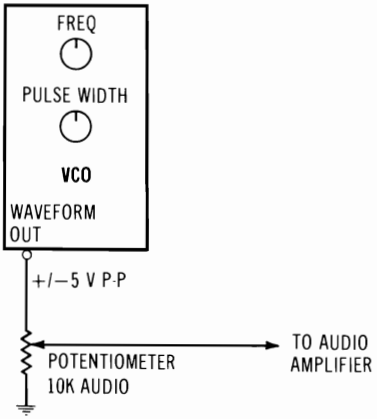



**Fig. 8-2. Using a potentiometer to reduce the signal level of a vco.**

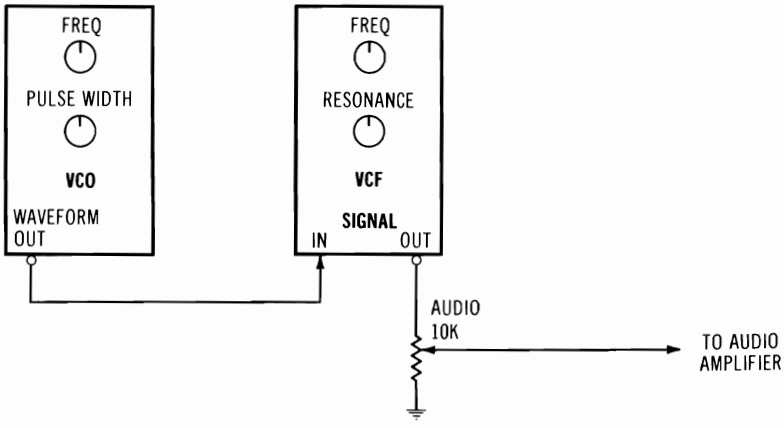



**Fig. 8-3. Using a vcf to filter a vco waveform.**

effect of increased resonance and, with some circuits, increase the resonance until the filter oscillates.

At this point you may wish to build the keyboard interface (or some other type of controller). Polyphonic keyboards are nice to have and will allow future system expansion, but they are usually very expensive. Most of us will get by with a one- or two-voice keyboard (monophonic or duophonic). With a keyboard and a properly calibrated vco, musical scales can be generated with the synthesizer (although the notes will not die out and will have an instant attack).

To add dynamics to the timbre and amplitude of the synthesizer sound, a vca and envelope generator can be constructed. The envelope generator output (triggered by the keyboard) can be used to control the cutoff of the vcf and the gain of the vca (see Fig. 8–4).

A second vco is a useful addition to the basic system. Its output can be summed with the other vco output to create the ensemble effect (richer sound due to the slight phase variations of the two oscillators). The two oscillators can be set to the same frequency or to integrals of each other for harmonically rich sounds (Fig. 8–5A). The two oscillators can also be synchronized, where phase variations are eliminated or reduced (Fig. 8–5B). Finally, one oscillator can function as a source of modulation; it can modulate the pulse width or frequency of the other vco (see Fig. 8–5C).

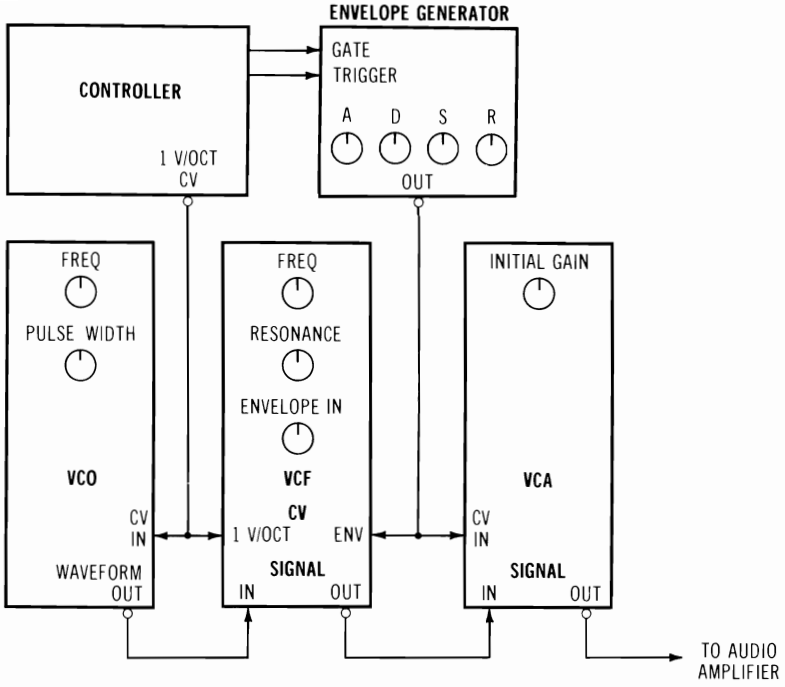
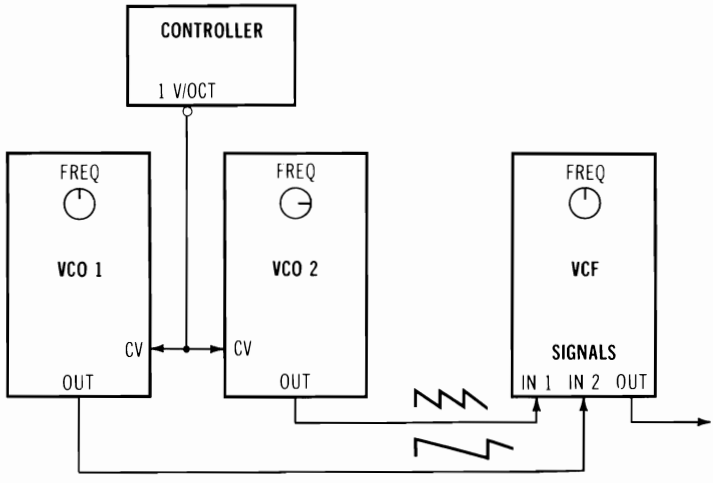



**Fig. 8-4. Adding an envelope generator, controller, and vca to the system.**

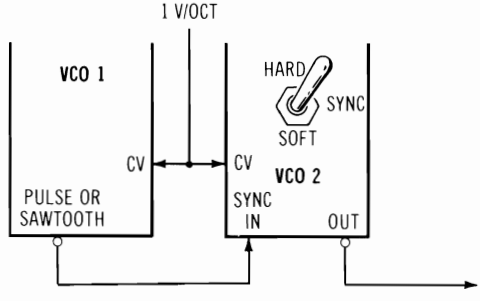
A second envelope generator may be desired to provide separate control over the timbre and amplitude of the sound. With the addition of a second vco and an envelope generator, the synthesizer can generate a large variety of sounds. Take time to familiarize yourself with the operation of the various module controls and functions before going on to further expansion.

## THE ADVANCED SYSTEM

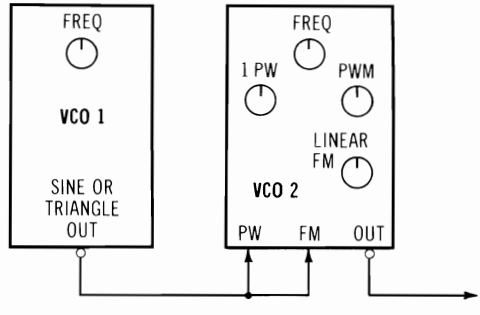
An advanced system is basically the previous basic system with options added such as additional vcf's, analog delay lines, sample and holds, lfo's, four-quadrant multipliers, etc. The order of importance of these additional modules depends on the sound the musician (programmer) wants to obtain. Several books and magazine articles have been written on the subject of synthesizer programming—obtaining the sound you want to




(A) Summing two vco signals with a two-input vcf.




(B) A patch for syncing two vco's.




(C) Using a vco to modulate frequency (FM) and pulse width (PW).

**Fig. 8-5. Some uses of two oscillators in a basic system.**

hear by various module interconnections and control settings (see *Polyphony* magazine, listed in Appendix A). Rather than our delving into this subject full tilt (which would triple the size of this book), the various modules will be described as to their use and possible placement in a "programmed" synthesizer patch.

### Controllers

Controllers can be used in a number of applications, as illustrated in Fig. 8–6. The joystick pressure-sensitive controller and ribbon controller can be used to generate a control voltage for a module. For example, the voltage generated by a ribbon controller can be summed with a keyboard 1 V/OCT at a vco, as in Fig. 8–6A. The voltage generated by such a controller can also be used to control a vca that generates a modulation waveform (Fig. 8–6B).

### Sequencers

Common uses of sequencers are shown in Fig. 8–7. Sequencers generate a control voltage that can be used to control another module's operation. They are commonly used to control the frequency of one or more vco's, to generate tone sequences. A sequencer can also be used to control a vca for rhythmic or percussive effects.

### Noise Sources

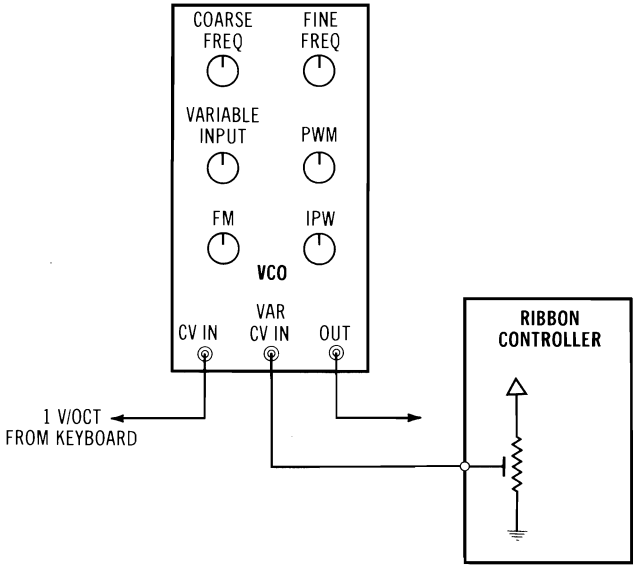
Noise sources are used with vcf's to generate whistle tones, cymbal sounds, or the common rain, surf, and wind sounds. The noise source can be used as a random modulation source for vcf's, vco's and vca's. Also, the noise source is often used with a sample and hold and lfo module to generate random control voltages. Two noise source applications are illustrated in Fig. 8–8.

### LFOs

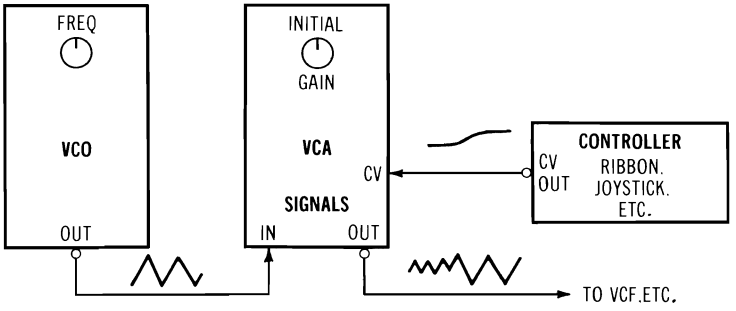
Lfo's act as valuable modulation sources for other modules (Fig. 8–9A). Often a triangle lfo is used to modulate the pulse width of a vco square wave. An lfo can also be used to sweep vcf's and to pan a signal between two vca's, as in Fig. 8–9B. The square wave output of an lfo can be used as a gate signal for sample and holds, vca's, or envelope generators.

## External Signal Processors

A synthesizer can be used to modify the timbre and dynamics of an externally audio signal, as in Fig. 8–10. A gate and trigger extractor derives timing signals from the audio signal's amplitude envelope. These timing signals can be used

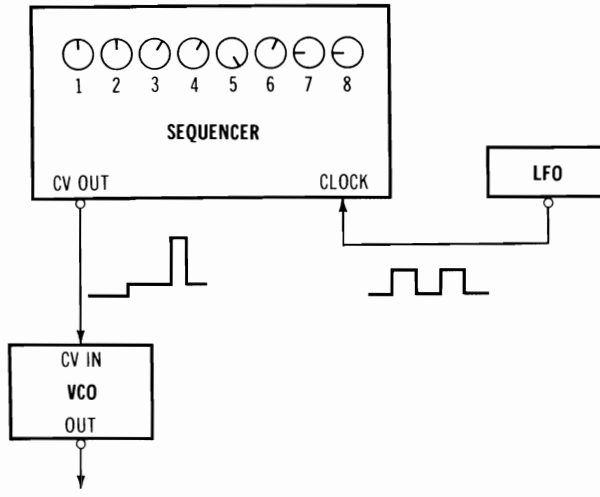



(A) Connecting a ribbon controller to the "variable" input of a vco (see circuit of Fig. 4-16).

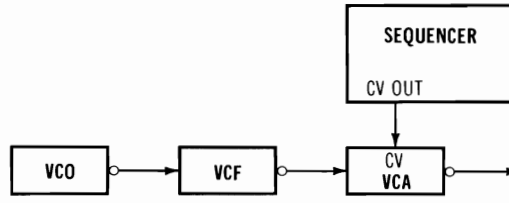



(B) A patch using a controller to affect the level of a modulation source.

**Fig. 8-6. Some uses of manual controllers in a basic system.**




(A) To control the frequency of a vco.



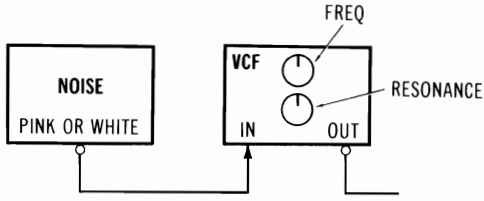

(B) To control the amplitude of a vca.

**Fig. 8-7. Some uses of a sequencer in a basic system.**

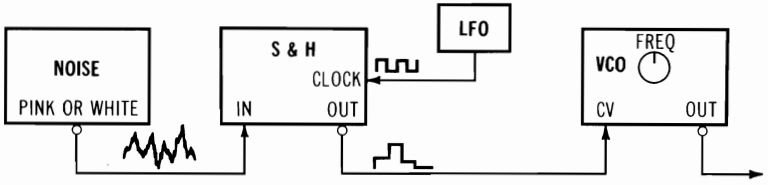
to trigger envelope generators. The amplitude envelope of the audio signal can be used as a control voltage for vcf's or vca's. Various vcf's, fixed filter banks, phasors, and/or timbre modulators can also be used to modify the signal's timbre. A four-quadrant multiplier can be used (audio signal on one input, vco output on the other input) to drastically alter the signal's pitch and tonality (see Fig. 8–11).

## Filter Modules

Generally, filters are wired directly to the output of the sound source(s), such as a vco, external audio, and the like, in a system patch (Fig. 8–12). Usually, as large a signal as possible is used with the filter, to obtain a respectable signal-to-noise ratio.

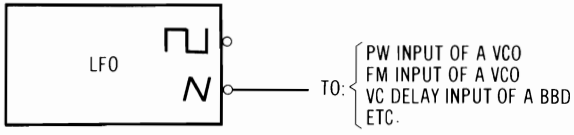



(A) A patch for wind and surf sounds (manually controlled).

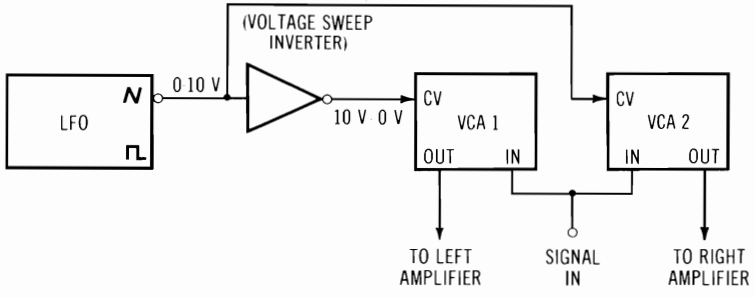



(B) A random tone patch.

**Fig. 8-8. Common uses of a noise source.**




(A) Modulation uses.




(B) Using a 0-to-10-V triangle output of lfo to pan a signal between two output amplifiers.

**Fig. 8-9. Some lfo uses.**

Pulse signals (from a sequencer, for example) can also be passed through a highly resonant vcf for percussion sounds. This is shown in Fig. 8–12B.

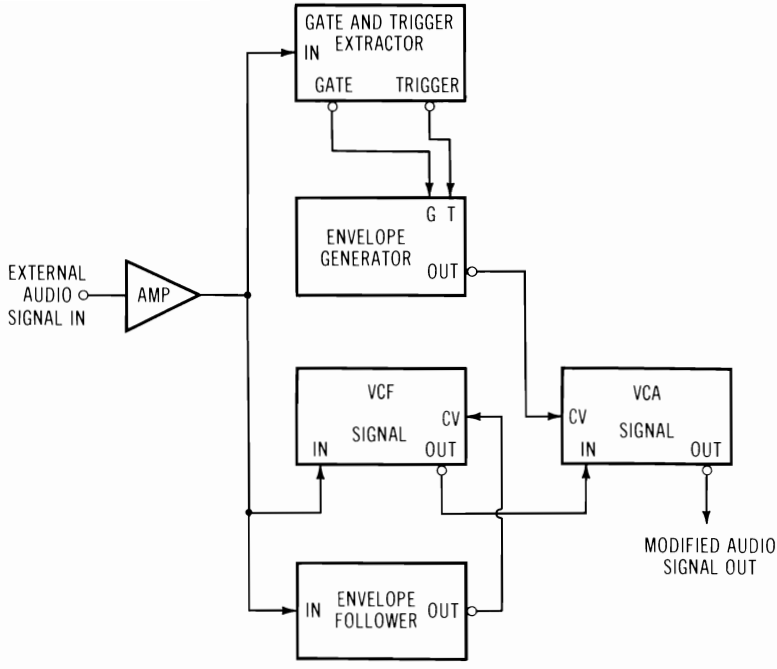



**Fig. 8-10. Using synthesizer modules with an external audio signal.**

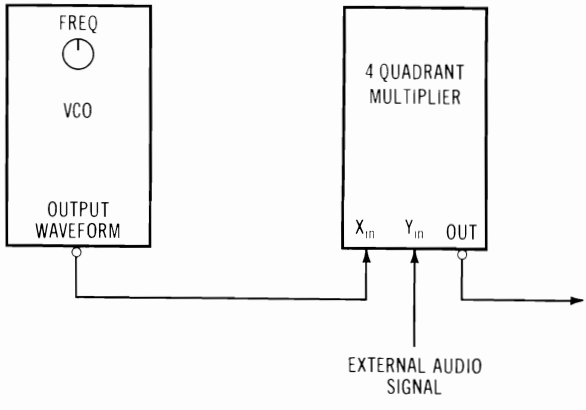
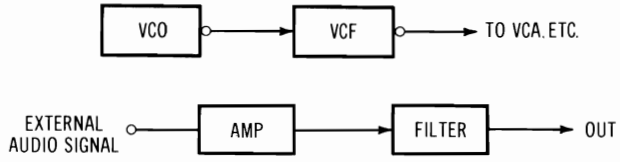
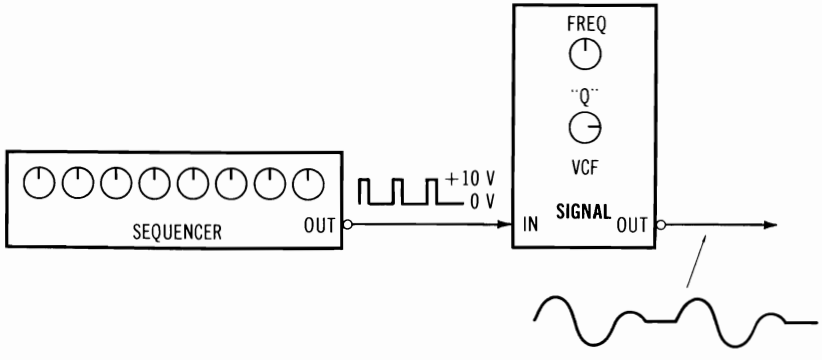



**Fig. 8-11. Using a four-quadrant multiplier to drastically modify the tonality of an audio signal.**




(A) The filter is usually placed directly after a sound source.




(B) "Ringing" a highly resonant filter with pulse signals.

**Fig. 8-12. Some common uses for filters.**

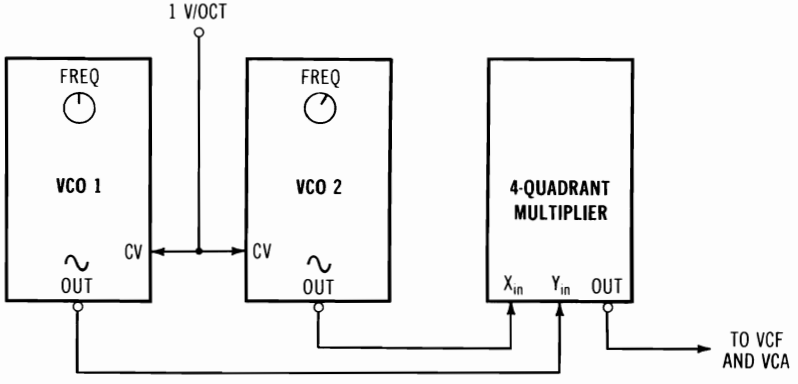



**Fig. 8-13. Creating bell sounds with two vco's and a four-quadrant multiplier.**

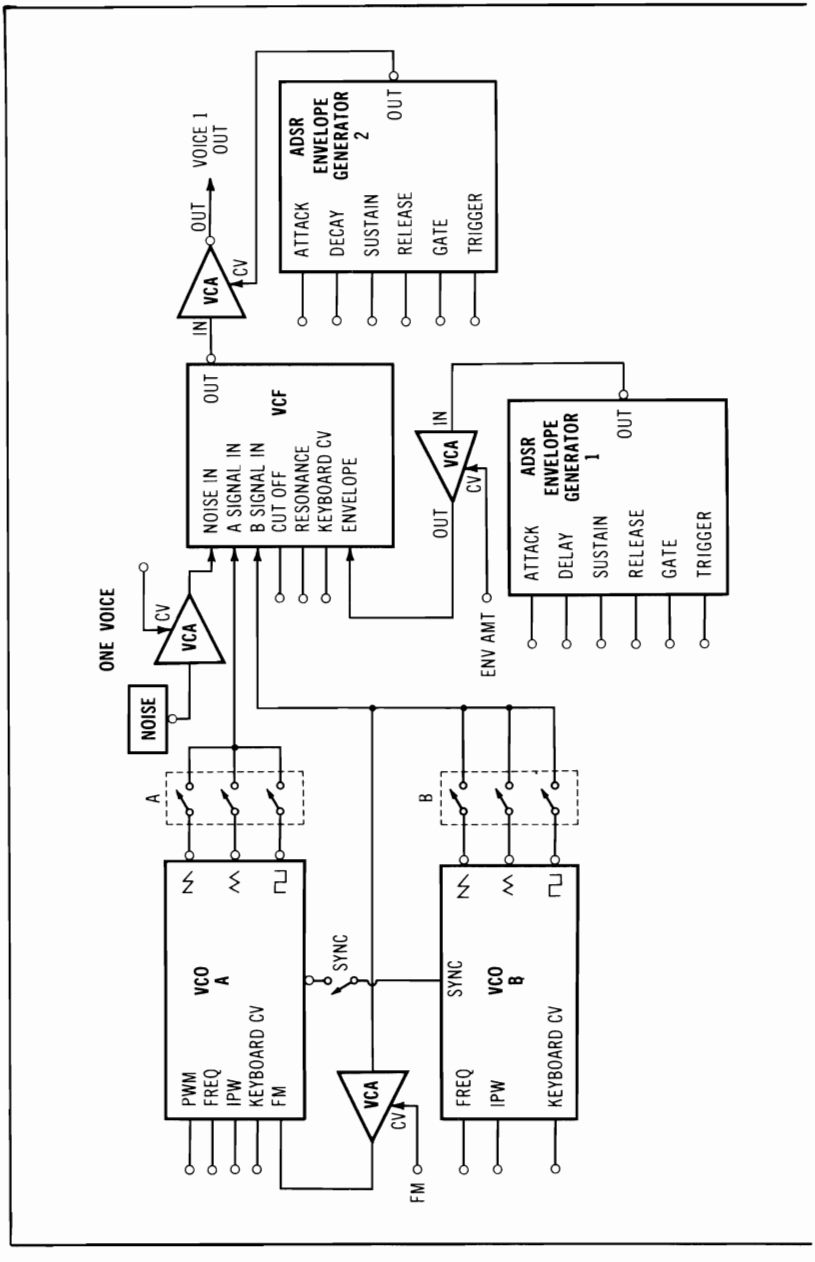
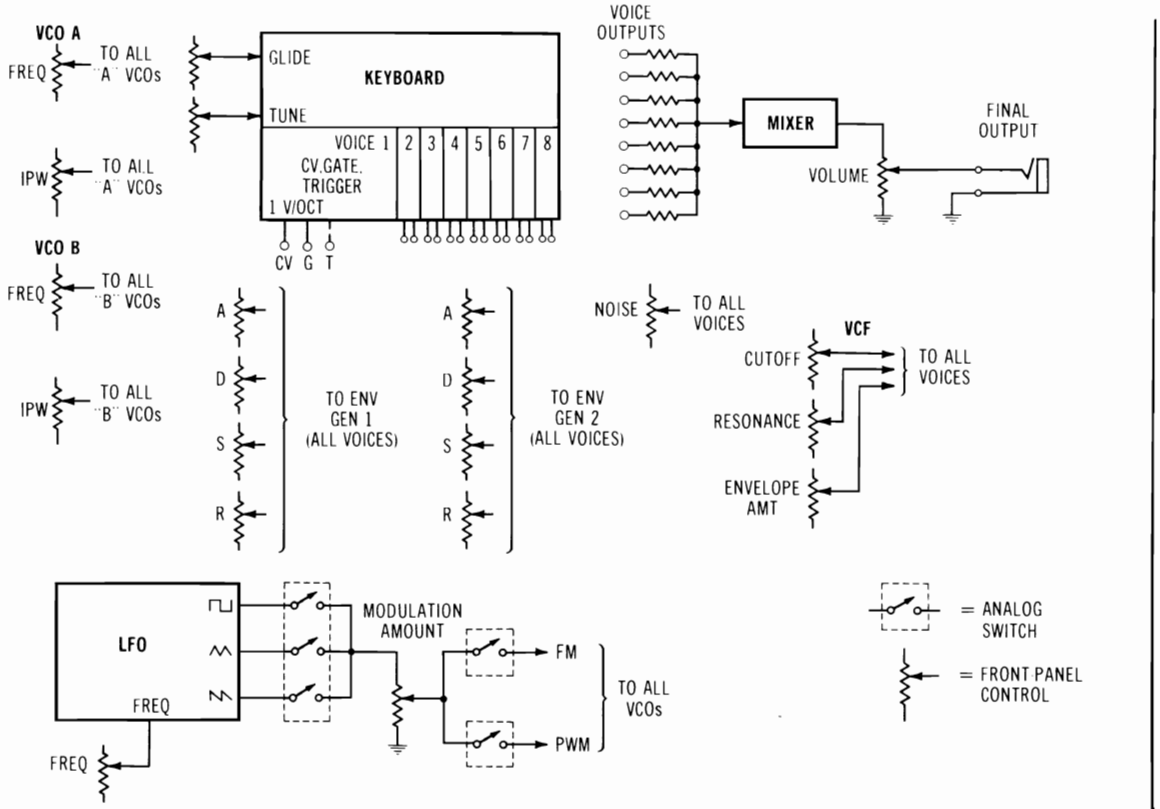



**Fig. 8-14. A typical**


VCO A
FREQ
TO ALL "A" VCOs
PW
TO ALL "A" VCOs
VCO B
FREQ
TO ALL "B" VCOs
PW
TO ALL "B" VCOs
GLIDE
KEYBOARD
TUNE
VOICE 1 2 3 4 5 6 7 8
CV.GATE. TRIGGER
1 V/OCT
CV G T
A
D
S
R
TO ENV GEN 1 (ALL VOICES)
A
D
S
R
TO ENV GEN 2 (ALL VOICES)
VOICE OUTPUTS
MIXER
FINAL OUTPUT
VOLUME
NOISE
TO ALL VOICES
VCF
CUTOFF
RESONANCE
ENVELOPE AMT
TO ALL VOICES
LFO
FREQ
FREQ
MODULATION AMOUNT
FM
PWM
TO ALL VCOs
= ANALOG SWITCH
= FRONT PANEL CONTROL

### Analog Multipliers

Voltage controlled amplifiers are used anywhere amplitude control is desired. They can be used in panning circuits and voltage controlled modulation circuits, and they have a multitude of other uses. In addition to modifying an external signal's tone characteristics, a four-quadrant multiplier can be used with two vco's to create interesting, sometimes bell-like, timbres (Fig. 8–13).

## THE POLYPHONIC SYSTEM

Polyphonic systems consist of several "voices," each similar to the expanded basic synthesizer discussed previously. A block diagram of a polyphonic system is shown in Fig. 8–14. As can be seen in this figure, the vcf and envelope generator functions of each voice receive the same control voltages to ensure uniformity of timbre and dynamics between voices. Custom ICs are common in these applications due to their low parts count and fairly well matched characteristics. Microcomputers are also used in polyphonic synthesizers to memorize patch settings, perform keyboard voltage and timing signals designations (voice priority), and keep the many vco's (generally eight or more) in tune. The hardware (circuitry) design of polyphonic synthesizers is now fairly straightforward, thanks to the many custom ICs available. More effort is currently placed on expanding a synthesizer's uses and capabilities through software (programmed sequences of instructions for the microcomputer to execute). With the introduction of microcomputers to electronic music, patches can be stored or recalled in seconds. Complex sequencer functions are relatively easy to implement. Truly, the next decade will be a very exciting one for electronic music enthusiasts.

# SYNTHESIZER CONSTRUCTION AIDS

# APPENDIX A

The purpose of this section is to aid the hobbyist in obtaining additional information, parts, and services that will aid him or her in constructing a synthesizer. Also, helpful information is given on making printed circuit boards and on circuit troubleshooting.

## SUGGESTED REFERENCE MATERIAL

It is very important for you to keep a current reference library of material on electronic music. This will aid you in designing new modules (or redesigning old ones) and keep you up to date with new technology advancements.

### Electronotes

*Electronotes* is an electronic music newsletter published (usually monthly) by Bernie Hutchins. This newsletter is *vital* in order to keep informed on the latest developments in electronic music technology. *Electronotes* is very circuit oriented, although it does occasionally delve heavily into mathematics. All circuits are fully described, and even if you don't want to build a circuit, you can learn a lot about the design concepts used. A *preferred circuits collection* is also available that is an updated collection of circuits published in *Electronotes*.

Electronotes
Bernie Hutchins
1 Pheasant Lane
Ithaca, NY 14850

### CFR Technotes

*CFR Technotes* is a newsletter dealing with electronic music circuitry. It has not been published for some time but may be back in print soon.

CFR Technotes
c/o CFR Associates, Inc.
Newton, NH 03858

### Electronics Today International (ETI) Magazine

*ETI Magazine* has continually offered very interesting construction articles dealing with a large variety of subjects, including electronic music (several complete synthesizer projects). The magazine is published in England and is highly recommended.

Modmags, Ltd.
145 Charing Cross Road
London WC2H OEE, U.K.

### Polyphony

*Polyphony* is a magazine that deals with system patch theory, new developments, and some circuit theory. The magazine is affiliated with PAIA Electronics.

Polyphony
P.O. Box 20305
Oklahoma City, OK 73156

In general the over-the-counter magazines available in the U.S. are devoid of electronic music circuits, compared with foreign publications. The writer suggests that you find a store that stocks the U.S. publications and buy an issue when it is worthwhile. Magazines devoted to amateur radio, such as *73* and *QST*, often contain useful circuit theory that can increase your electronics knowledge.

### Engineering Magazines

Technical publications aimed at electrical engineers can contain useful circuit information and theory, which can be applied

to electronic sheet music. Many contain a reader submitted "circuit designs" section that is often valuable.

EDN
270 St. Paul St.
Denver, CO 80206

Electronic Design
50 Essex St.
Rochelle Park, NJ 07662

Electronics
1221 Ave. of the Americas
New York, NY 10020

### Contemporary Keyboard Magazine

*Contemporary Keyboard Magazine* is a magazine devoted to keyboard instruments and players in general. It usually contains one or more columns dealing with system patch theory.

Contemporary Keyboard
GPI Publications
Box 615
Saratoga, CA 95070

### IC Cookbooks

Several books are available that detail uses of CMOS, TTL, and linear ICs. Some useful books of this type include:


1. Berlin, H.M., *Design of Op-Amp Circuits, With Experiments.* Indianapolis: Howard W. Sams & Co., Inc., 1978.
2. Lancaster, D., *The TTL Cookbook.* Indianapolis: Howard W. Sams & Co., Inc., 1974.
3. Berlin, H.M., *Guide to CMOS Basics, Circuits, & Experiments.* Indianapolis: Howard W. Sams & Co., Inc., 1979.
4. Berlin, H.M., *Design of Active Filters, With Experiments.* Indianapolis: Howard W. Sams & Co., Inc., 1978.
5. Jung, W., *The Op-Amp Cookbook.* 2nd ed. Indianapolis: Howard W. Sams & Co., Inc., 1980.


### IC Manufacturer's Data Books/Application Notes

Several IC manufacturers offer data books that contain reference data on their ICs as well as application notes. Some suggested application books are the following:

National Semiconductor Corp., 2900 Semiconductor Drive, Santa Clara, CA 95051:
*Linear Applications Handbook*
*Voltage Regulator Handbook*
*Audio/Radio Handbook*

Analog Devices, Inc., Norwood, MA 02062:
*Nonlinear Circuits Handbook*

Signetics, P.O. Box 9052, 811 East Arques Ave., Sunnyvale, CA 94086:
*Analog Applications Manual*

IC data books can be obtained direct from the manufacturer or from their local distributors (usually listed in the phone book).

## SYNTHESIZER KITS

Several companies offer synthesizer modules/units in kit form. If you do not have a lot of time to design circuits, lay out pc boards, and obtain parts, this may be the way to go.

### PAIA Electronics

PAIA Electronics produces a large variety of electronic music kits, including a modular synthesizer kit that can be interfaced with a computer. They also have a series of projects using the recently available custom ICs (including a 16 preset programmable synthesizer for under $500). Many products are available assembled.

PAIA Electronics, Inc.
1020 W. Wilshire Blvd.
Oklahoma City, OK 73116

### Aries

Rivera Music Services now markets the Aries modular synthesizer kits. This line consists of a large variety of modules.

Rivera Music Services
49 Brighton Ave., No. 11
Boston, MA 02134

### Applied Synergy

Applied Synergy has a complete line of services and products for the hobbyist. These include circuit boards for custom ICs, a polyphonic keyboard, silk-screening and panel construction, custom modifications, and more.

Applied Synergy
311 West Mifflin St.
Lancaster, PA 17603

### Powertran

Powertran has several synthesizers and a vocoder available in kit form. Many of these circuits were published in *ETI Magazine.*

Powertran
Portway Industrial Estate
Andover, Hants SP10 3NM U.K.

### Digisound

Digisound has a complete line of synthesizer module kits (including some circuits in this book). They also offer a construction manual for a complete system.

Digisound, Ltd.
13 The Brooklands
Wrea Green, Preston
Lancashire PR4 2NQ U.K.

### CFR Associates

CFR Associates has several synthesizer module kits available.

CFR Associates
Newton, NH 03858

### Serge Modular Music Systems

Serge has a large variety of unique synthesizer modules available in kit or assembled form.

Serge Modular
572 Haight St.
San Francisco, CA 94117

### Maplin Electronic Supplies, Ltd.

Maplin has a large line of products in kit form (including synthesizers).

Maplin Electronic Supplies, Ltd.
P.O. Box 3
Rayleigh, Essex SS6 8LR
United Kingdom

### E-mu Systems

E-mu Systems is a manufacturer of large modular studio synthesizers. They offer several "submodules" which are preassembled circuit boards that function as the heart of a synthesizer. E-mu also publishes a nice technical catalog of their products.

E-mu Systems
417 Broadway
Santa Cruz, CA 95060

## PARTS

Many of the components used in this book can't be found in your neighborhood electronics store. Resistors, capacitors, and the majority of ICs can be obtained from advertisers in the various electronics magazines. Because of this, it is a good idea to collect catalogs from many suppliers. And always remember: buyer, beware.

### Custom ICs

The following are addresses of suppliers of custom ICs used in circuits in this book:

*Curtis ICs*

Curtis Electromusic Specialties
110 Highland Ave.
Los Gatos, CA 95030

PAIA Electronics (also a source for keyboards)

Digisound, Ltd. (also a source for tempco resistors)

*Solid State Micro Technology for Music, Inc.* (SSM)

Solid State Micro Technology for Music, Inc.
2076B Walsh Ave.
Santa Clara, CA 95050

Digisound Ltd.

E-mu Systems (small quantities only)

*B & B Audio*

Aphex Systems, Ltd.
7801 Melrose Avenue
Los Angeles, CA 90046

## BUILDING A SYNTHESIZER

### Test Equipment Required

Not too much is required in the form of test equipment to get a synthesizer up and running. Many of the adjustments can be done by ear.

An *oscilloscope* is just about a necessity. An inexpensive scope is all that is required, as we are generally working with signals under 20 kHz.

A *dvm* (digital voltmeter) is nice to have also. However, an analog meter (vom) will do for many applications. A high-precision dvm is useful when you wish to measure microampere currents, match resistors to 1 percent or less, or adjust precision circuits.

A *solderless breadboard* (such as those manufactured by Global Specialties Corp., A.P. Products, and E&L Instruments, Inc.) is very handy for testing new designs. Buy several so you don't run out of space in the middle of a design.

A power supply is absolutely necessary. Simple circuits, such as those given in Chapter 2, are sufficient. You will need ± 15 V for analog and CMOS circuitry and +5 V for any TTL circuitry.

### Making Your Own Printed Circuit Boards

If you wish to make your own pc boards, the following method is the fastest the writer has found. First, buy some 0.1-inch grid graph paper (0.1 in × 0.1 in, or 0.25 × 0.25 cm). This

paper should be fairly thin, with blue grid lines. You also need to buy several *permanent-ink*, fine-point, felt-tipped markers.

Back home, it is time to lay out your circuit board on the graph paper. Tape a sheet of white paper to your desk top. Then tape a sheet of the graph paper over this. The blue grid lines should now stand out. The next part is the hard part. If you like jigsaw puzzles, you will enjoy laying out pc boards. When you are laying out a board, the following rules should be abided by:

1. Make supply and ground traces as large as possible.
2. Bypass supply lines to ground with 0.1-$\mu$F ceramic capacitors in several places on the circuit board (by each IC is great) (Fig. A-1).
3. Where the supply lines attach to the pc board, install 0.1-$\mu$F or larger tantalum capacitors between the supply voltages and ground (Fig. A-2).
4. Keep op-amp summing node ("−" input) traces short. Making these long will invite oscillation, rf pickup, and noise. Also, keep in mind the suggested guarding method for sample and hold circuits (given in Chapter 3).
5. Try and avoid ground loops by using a single-point ground (all ground connections go to a single point), or by organizing ICs according to signal flow. Those ICs closest to the module input should be farthest away from the external supply connections. Those ICs close to the module output can go closer to the external supply connections (Fig. A-3).

Get out a couple of your electronic magazines and take a look at how they designed their pc boards. Don't be afraid to add jumpers where necessary. This writer has found that the best procedure is to lay out a board using the symbols shown in Fig. A-4 for ICs, resistors, capacitors, and jumpers. Use dots for holes. Connect the dots with a single line. You should be able to space lines on the pc board 0.1 inch (0.25 cm) apart with no problem. Note that the layout is done from a topside view.

Once you have finished the layout with the permanent-ink marker, cut a piece of circuit board to size and tape the grid paper layout over the fiberglass side. Cover the grid paper layout with invisible-type tape. This is to protect it from damage during the next step.

Now it is time to drill the board. A good size drill bit to use is a No. 60. Drill holes everywhere you see a dot in the layout.

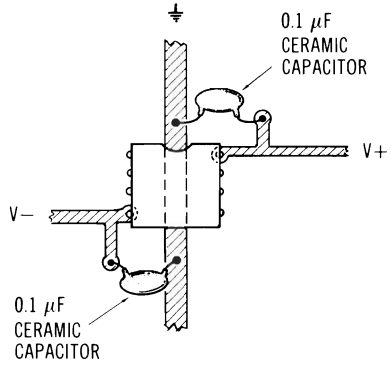



**Fig. A-1. Bypassing IC with ceramic capacitors.**

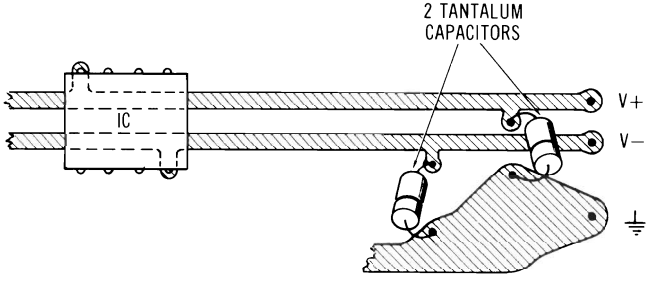
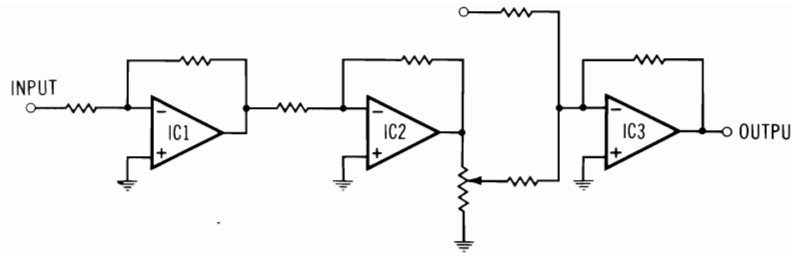



**Fig. A-2. Bypassing external supply connections.**

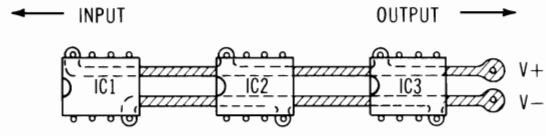
Once you are sure you have drilled them all, carefully remove the layout from the pc board. Hold the layout up to the light to see if you missed any holes. If you did, stick the layout back on the board and drill the remaining holes. Save the layout as a reference of all circuit traces on the board.

Use a blunt metal edge of some type to scrape off burrs surrounding the holes on the copper side of the pc board. Once this is done, you should clean the copper with steel wool or a powder cleanser and water until it has a bright shine. Make sure it is clean of dirt, corrosion, and fingerprints.

Turn the layout *upside down* on the white paper taped on your desk. You should be able to see the circuit traces through the paper. Now you can use the felt-tipped pen to draw the circuit traces on the pc board, using the upside-down drawing for a reference. If you make a mistake, you can use a pencil eraser or




(A) Simple circuit example.



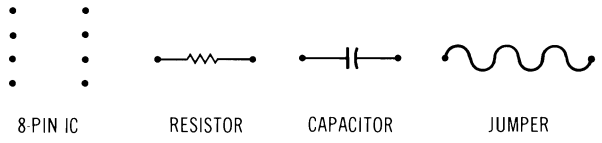

BYPASS CAPS OMITTED FOR CLARITY

(B) Sample pc layout of ICs.

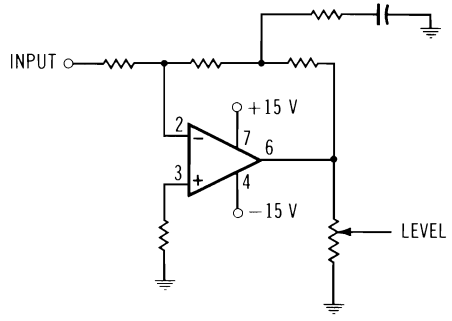
**Fig. A-3. A simple circuit and its pc layout (ICs only).**

small knife to remove the ink. Be sure that the ink is going on thick and black. Don't be miserly with the pens or you will regret it when you see your finished board.

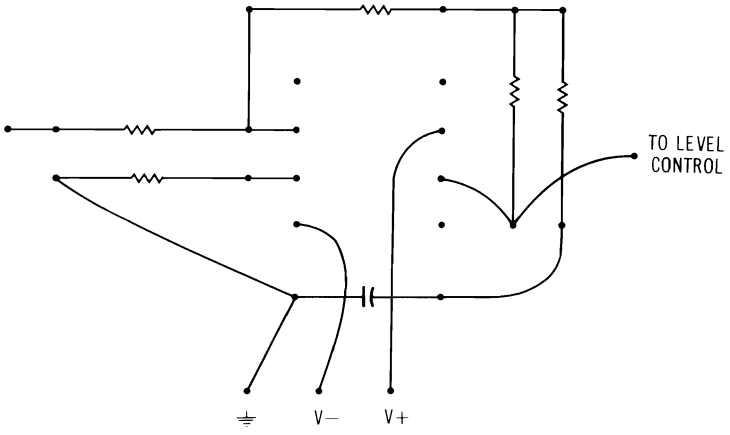
After you have finished drawing the circuit with the pen, you can etch the board. Ferric chloride is the most popular chemical for this purpose. It can be obtained as a solid which you dissolve in water or as a solution from most chemical supply houses (at a cost much less than at your electronic store). The etching process should be done at a location far away from everyone and everything. The fumes will etch metal, so guess what they do to your lungs. Wear old clothes when etching your boards. Ferric chloride stains will not come out. The actual etching is best done in a Pyrex (glass) cooking tray. Pour about an inch of etch into the tray. Place your boards copper side down on top of the etch (so they float). If the board sinks, you will probably have to turn it over, let it sink, and agitate the tray until the board is etched. If your board floats, you can leave it there for 10 to 20 minutes and let it etch. A floodlight placed over the board will heat it and the etch and speed up the etching time, or the Pyrex tray could be put on a hot plate set on its lowest heat setting.




(A) Component symbols.




(B) A simple circuit.




(C) A sample layout for (B).

**Fig. A-4. Laying out a pc board.**

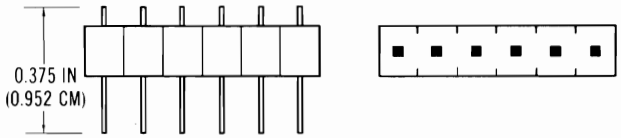
After the board is finished etching, clean it with water and then steel wool. You may see places where the copper did not etch due to air bubbles. These spots can usually be cleaned up with a knife.

If you wish to make another board, re-cover the top side of the layout with tape. This is so you can tell if you have drilled all the holes when you use it again.

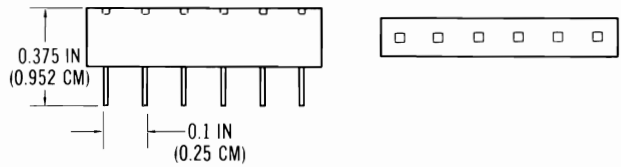
When you have finished with the etch, pour it back into the container. It can be reused many times. *Never pour the etch down the sink*, as it can etch through pipe.

## MODULE CONSTRUCTION

You should build your synthesizer in modules. Each module will consist of a front panel and a circuit board. Patch connections are made with ¼-inch phone jacks. Each module will require some type of connector to interface with the main system power supply. In-line connectors similar to those used in radio control systems for airplanes can be used. Connectors called "headers" (such as those made by AP Products) can be bought in long strips and cut down to the size we need (generally four-conductor, Fig. A-5).




(A) Male header connector.




(B) Female header connector.

**Fig. A-5. Header connectors used for power supply connections.**

Use the thickest sheet aluminum you can find or afford for the front panels. Metal salvage yards are a good source for small sheets (usually sold by the pound). Have it sheared into several 3-inch by 9-inch (7.6- by 22.8-cm) pieces.

You may wish to tape some of the 0.1-inch grid paper (the same type used in the pc layout process) over the panel to help you center the holes. Suggested hole spacings are given in Fig.

A-6. Cover the grid paper with invisible tape to make it durable and reusable for additional panels. Mark the hole locations through the paper and into the aluminum with a punch or nail. Remove the paper and drill the holes. It is the best to start out with small drill bits and work up to the final bit size. You can deburr the drill holes with a larger-size drill bit.

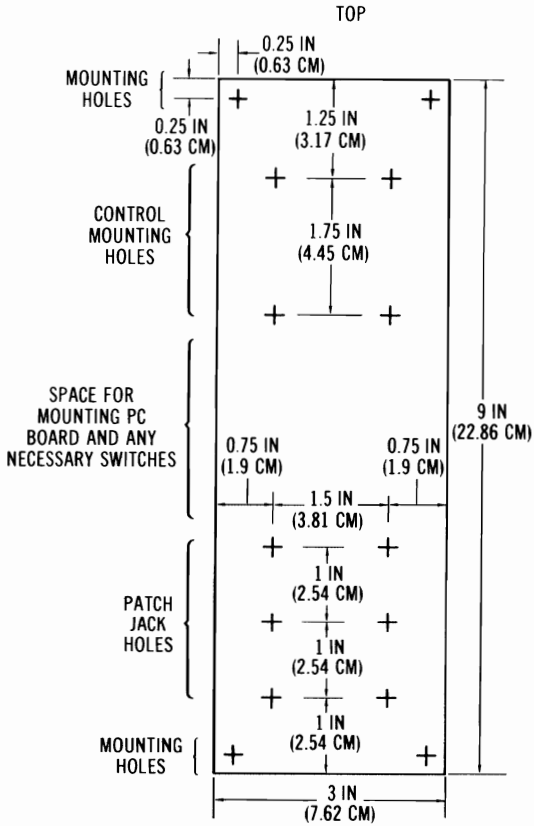



**Fig. A-6. The front panel.**

Once all the holes are drilled, you can "frost" the front side of the panel with a wire-brush "grinding" wheel. This gives the panel a nice appearance and removes any corrosion marks on the aluminum.

A piece of sheet metal bent in a 90° angle can be used to mount the circuit board. Leave an extra ½ inch (1.27 cm) on the

circuit board to allow for mounting. You can also use pieces of aluminum "L" channel to mount your board. Pop-rivets or screws can be used to mount the channel pieces to the front panel. Both methods are shown in Fig. A-7.

Rub-on letters can be used to label your front panels, but they take a lot of time and effort. You might try a hand labeler (Dymo or equivalent) for a quick and easy method. It doesn't look too bad either.

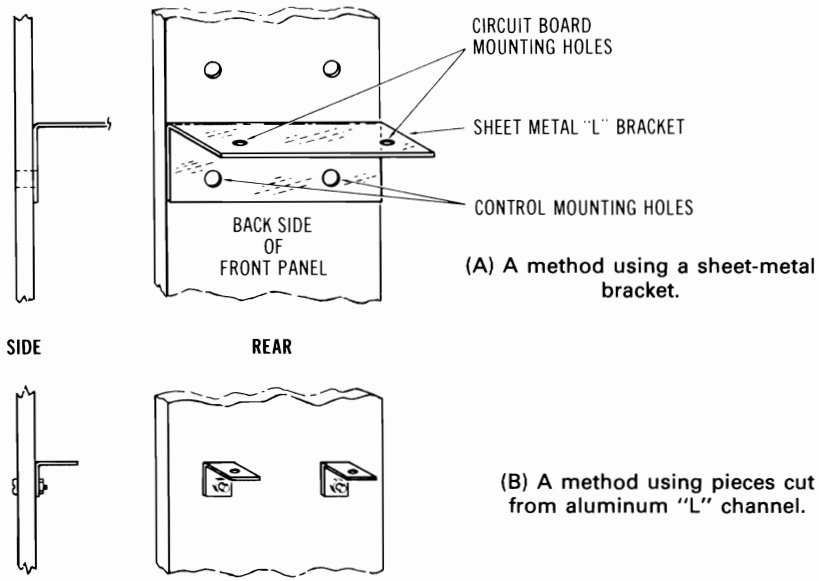

CIRCUIT BOARD MOUNTING HOLES
SHEET METAL "L" BRACKET
CONTROL MOUNTING HOLES
BACK SIDE OF FRONT PANEL
(A) A method using a sheet-metal bracket.
SIDE
REAR
(B) A method using pieces cut from aluminum "L" channel.

**Fig. A-7. Methods of mounting the pc board to the front panel.**

## Testing the Module

Major causes of nonfunctional circuits will be: an error in the pc board layout, power supply disconnected or not turned on (don't laugh), or bad ICs. I suggest that you use sockets for your ICs. If you find them too expensive, use Molex pins (these come in strips and are like sockets without the plastic casing). You may want to check out your op amps on your prototyping board first, if you doubt that they are good. To do this wire them up as simple unity-gain amplifiers.

Install the ICs and turn on the power. If the module does not work, try to troubleshoot the circuit one section at a time,

possibly starting at the control voltage section. Get as much of the circuit working as you can. If you are using a custom IC, check out all of the external circuitry. If that seems to check out satisfactory, try testing the custom IC on your prototyping board.

You may experience unwanted oscillations in some of the op-amp circuits. This is more likely to occur with the FET-input op amps. Try installing small-value (10–50 pF) capacitors across the op amp feedback loop. This will reduce the high-frequency gain and possibly stop the oscillation. Other causes can be ground loops or long unshielded lines coming from the IC inputs.

### The Cabinet

You can make a cabinet for your synthesizer using 1-inch by 10-inch (2.54- by 25.4-cm) pine. See Fig. A-8 for some suggestions.

The modules are installed using small pan-head sheet-metal screws. Start out with just two screws per panel until you are sure you have all of the modules situated where you want them.

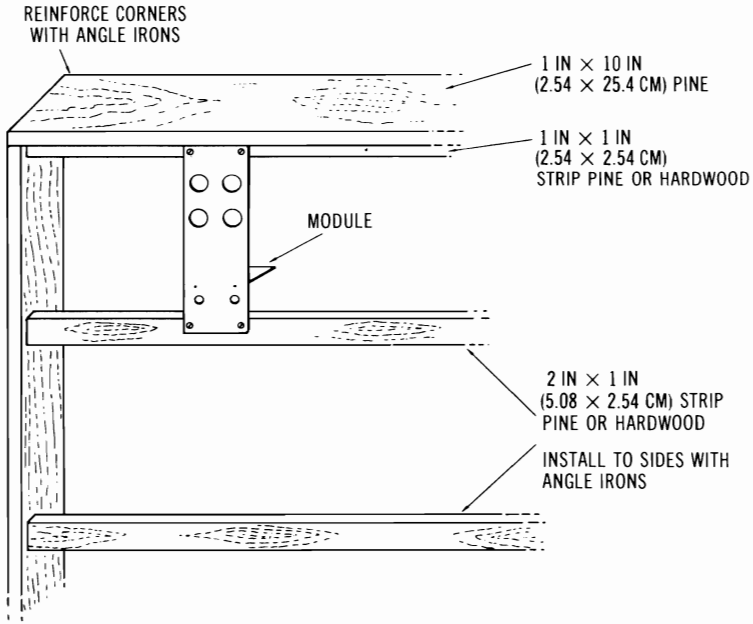

REINFORCE CORNERS WITH ANGLE IRONS
1 IN × 10 IN (2.54 × 25.4 CM) PINE
1 IN × 1 IN (2.54 × 2.54 CM) STRIP PINE OR HARDWOOD
MODULE
2 IN × 1 IN (5.08 × 2.54 CM) STRIP PINE OR HARDWOOD
INSTALL TO SIDES WITH ANGLE IRONS

**Fig. A-8. Some suggestions for cabinet construction.**

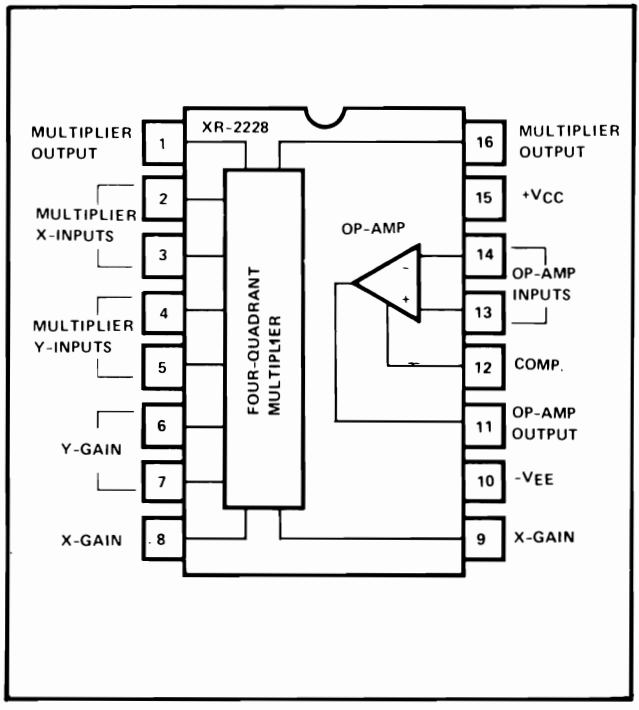
# IC DATA SHEETS AND PIN DIAGRAMS

# APPENDIX B

The material in this appendix has been provided as follows:

Page 235, courtesy Exar Integrated Systems, Inc.
Page 236, courtesy Signetics Corp.
Pages 237–248, courtesy Matsushita Electronics Corp.
Pages 249–265, courtesy Reticon Corp.
Pages 266–269, and 277–296, courtesy Curtis Electromusic Specialties.
Pages 270–276, courtesy Solid State Micro Technology for Music, Inc.

# FUNCTIONAL BLOCK DIAGRAM



## DESCRIPTION

The 570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The 570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

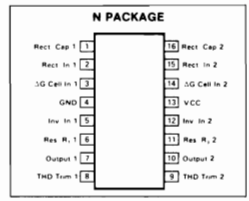
## FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

## APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

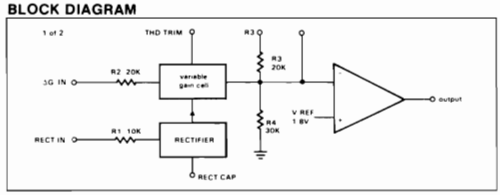
## PIN CONFIGURATION




## ABSOLUTE MAXIMUM RATINGS

| | PARAMETER | RATING | UNIT |
|---|---|---|---|
| | Positive supply | | Vdc |
| | 570 | 24 | |
| | 571 | 18 | |
| $T_A$ | Operating temperature range | -40 to +70 | °C |
| $P_D$ | Power dissipation | 400 | mW |

## BLOCK DIAGRAM




## CIRCUIT DESCRIPTION

The 570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at $V_{REF}$. The rectified current is averaged on an external filter capacitor tied to the $C_{RECT}$ terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G = \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

$$G = \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\quad \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio $I_{OUT}/I_{IN}$ controlled by the rectifier. $I_{IN}$ is the current which flows from the ΔG input to an internal summing node biased at $V_{REF}$. The following equation applies for capacitively coupled inputs. The output current, $I_{OUT}$, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_1} \approx \frac{V_{IN}}{R_1}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

The operational amplifier (which is internally compensated) has the non-inverting input tied to $V_{REF}$, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, $R_3$, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components. The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

Panasonic BBD Panasonic

# BUCKET BRIGADE DEVICES DATA

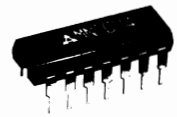
**MN3004**

## LOW NOISE 512-STAGE BBD FOR AUDIO SIGNAL DELAYS

**APPLICATIONS:**

The MN3004 is suitable for audio signal processing, e.g.;

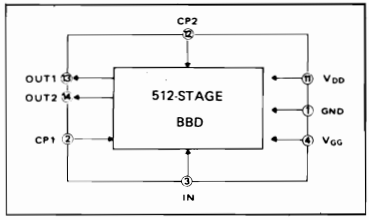
- Variable speech control of playback and voice control of tape recorders
- Reverberation effect of stereo equipments
- Tremolo, vibrato and/or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Telephone time compression and voice scrambling in communication systems; etc.



14-Lead Dual-In-Line Plastic Package

The MN3004 is a 512-stage Bucket Brigade Device (BBD).
A pair of output terminals is provided in the BBD for cancellation of the clock component superposed on the output signals.
P-channel silicon gate technology is used to fabricate the BBD into chains of tetrode-type MOS transistors and storage capacitors. The MN3004 is packaged in the standard 14-lead dual-in-line plastic package.

**BLOCK DIAGRAM**




**FEATURES:**

- Variable delay line in audio frequency range
- P-channel silicon gate, tetrode MOS transistors configuration
- Clock component cancellation capability
- Low insertion loss: 1.5 dB typ.
- Wide dynamic range: S/N ≃ 85 dB typ.
- Wide frequency response: $f_{in} < 12$kHz
- Low noise: 100 μVrms typ.
- Low distortion: 2.5% max.
- Clock frequency range: 10 ~ 100 kHz

The device specifications are subject to change for improvement without prior notice.

While every precaution has been taken in the preparation of this data sheet, the publisher assumes no responsibility for patent liability with respect to the use of the information contained herein.

**MATSUSHITA ELECTRONICS CORPORATION** SEMICONDUCTOR DIVISION

## ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Terminal Voltage | $V_{DD}$ $V_{GG}$ $V_{CP}$ $V_{IN}$ | −18 ~ +0.3 | V |
| Output Voltage | $V_{OUT}$ | −18 ~ +0.3 | V |
| Operating Temperature | Topr | −20 ~ +60 | ℃ |
| Storage Temperature | Tstg | −55 ~ +125 | ℃ |

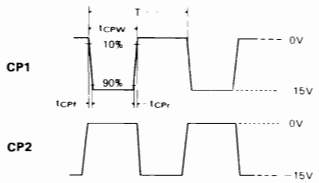
## OPERATING CONDITIONS (Ta = 25℃)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Drain Supply Voltage | $V_{DD}$ | | −14 | −15 | −16 | V |
| Gate Supply Voltage | $V_{GG}$ | | | $V_{DD}+1$ | | V |
| Clock Voltage "H" | $V_{CPH}$ | | 0 | | 1 | V |
| Clock Voltage "L" | $V_{CPL}$ | | | $V_{DD}$ | | V |
| Clock Input Capacitance | $C_{CP}$ | | | | 350 | pF |
| Clock Frequency | $f_{CP}$ | | 10 | | 100 | kHz |
| Clock Pulse Width *1 | $t_{CPW}$ | | | | 0.5T *2 | |
| Clock Rise Time *1 | $t_{CPr}$ | | | | 500 | nsec |
| Clock Fall Time *1 | $t_{CPf}$ | | | | 500 | nsec |

## ELECTRICAL CHARACTERISTICS (Ta = 25℃, $V_{DD}$ = $V_{CPL}$ = −15V, $V_{CPH}$ = 0V, $V_{GG}$ = −14V, $R_L$ = 100kΩ)

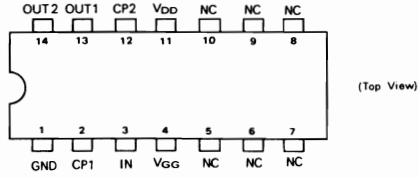
| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Signal Delay Time | $t_D$ | | 2.56 | | 25.6 | msec |
| Input Signal Frequency | $f_{in}$ | $f_{CP}$ 40kHz, 3dB down | | | 12 | kHz |
| Input Signal Swing | $V_{in}$ | 2.5% Distortion | | | 1.8 | Vrms |
| Insertion Loss | LI | $f_{CP}$ 40kHz, $f_{in}$ 1kHz | | 1.5 | 4 | dB |
| Total Harmonic Distortion | THD | $f_{CP}$ 40kHz, $f_{in}$ 1kHz<br>$V_{in}$ 0.78 Vrms | | 0.4 | | % |
| Noise Level | $V_N$ | $f_{CP}$ 100kHz<br>Weighted by "A" curve | | | 0.21 | mVrms |
| Signal to Noise Ratio | S/N | Max. Output Voltage<br>vs. Noise Voltage | 75 | 85 | | dB |

*1 Clock Waveforms

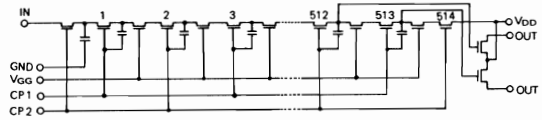



*2 T = 1/$f_{CP}$ (Clock period)

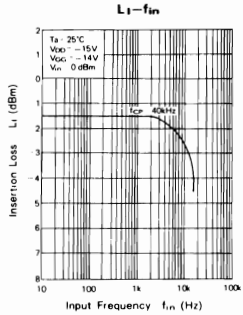
**TERMINAL ASSIGNMENTS**

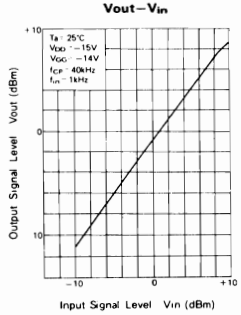


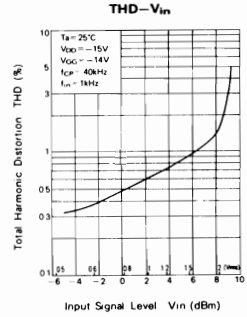

**CIRCUIT DIAGRAM**



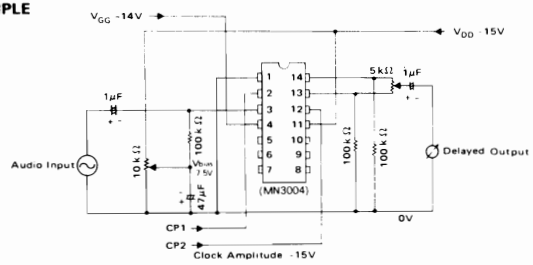

**TYPICAL CHARACTERISTICS** (Ta = 25℃)



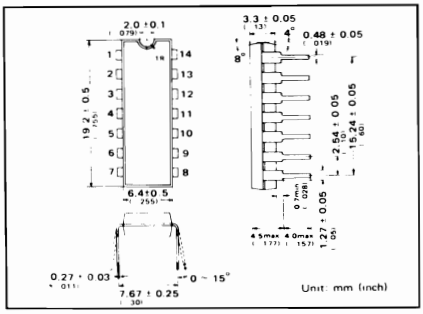



## CIRCUIT EXAMPLE




BASIC CIRCUIT WITH CLOCK COMPONENT CANCELLATION.

## OUTLINE DIMENSIONS




14 Lead Dual In Line Plastic Package

**MATSUSHITA ELECTRONICS CORPORATION**
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# DIGITAL INTEGRATED CIRCUITS PRELIMINARY DATA

# MN3101

## Clock Generator / Driver for BBD's

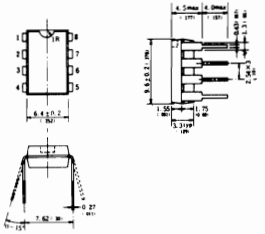
The MN3101 is a CMOS integrated circuit designed to generate low impedance two clock phases required for driving BBD's. In addition, the MN3101 provides the optimum $V_{GG}$ for BBD's* when the MN3101 is used with BBD's on a common $V_{DD}$ supply.

The self-contained oscillator can be controlled by an external R,C circuit, but an external oscillator can also be used. The clock frequency is 1/2 of the oscillation frequency.

* Matsushita Electronics Corporation's BBD product range: MN3001, MN3002, MN3003, MN3004, MN3005, MN3006, MN3007, MN3008, MN3009, MN3010, MN3011 (Developmental)

Note: The MN3003 is provided with an internal oscillator.

Unit: mm (inch)



8-Lead Dual-In-Line Plastic Package

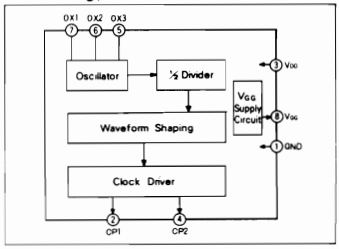
### Features:

- BBD direct driving capability—up to two MN3005 types (equivalent to 8192 stages).
- Either internal or external oscillator can be used
- Two phases (1/2 duty) output
- Provided with $V_{GG}$ supply circuit
- Operates on a single power supply: −8 ~ −16V
- 8-lead dual-in-line plastic package

### Application

- BBD clock generator / driver

### Block Diagram




The device specifications are subject to change without prior notice. While every precaution has been taken in the preparation of this data sheet, the publisher assumes no responsibility for patent liability with respect to the use of the information contained herein.

## Absolute Maximum Ratings (Ta=25°C)

| Item | Symbol | Ratings | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ | −18~+0.3 * | V |
| Input Terminal Voltage | $V_I$ | $V_{DD}$−0.3~+0.3 * | V |
| Output Terminal Voltage | $V_O$ | $V_{DD}$−0.3~+0.3 * | V |
| Power Dissipation | $P_D$ | 200 | mW |
| Operating Temperature | Topr | −10~+70 | °C |
| Storage Temperature | Tstg | −30~+125 | °C |

* With respect to GND=0V

## Operating Conditions

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | GND=0V | −8 | −15 | −16 | V |

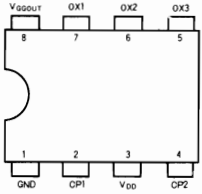
## Electrical Characteristics (Ta=25°C, $V_{DD}$=−15V, GND=0V)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{DD}$ | Without load | | 3 | | mA |
| Power Consumption | Ptot | Clock output 40kHz | | 45 | | mW |
| OX1 Input Terminal | | | | | | |
| Input Voltage "H" Level | $V_{IH}$ | | 0 | | −1 | V |
| Input Voltage "L" Level | $V_{IL}$ | | $V_{DD}$+1 | | $V_{DD}$ | V |
| Input Leakage Current | $I_{LK}$ | $V_I$=0~−15V | | | 30 | μA |
| OX2 Output Terminal | | | | | | |
| Output Current "H" Level | $I_{OH1}$ | $V_O$=−1.0V | 0.6 | | | mA |
| Output Current "L" Level | $I_{OL1}$ | $V_O$=−14V | 0.5 | | | mA |
| Output Leakage Current | $I_{LOL1}$ | $V_O$=$V_{DD}$ | | | 30 | μA |
| Output Leakage Current | $I_{LOH1}$ | $V_O$=GND | | | 30 | μA |
| OX3 Output Terminal | | | | | | |
| Output Current "H" Level | $I_{OH2}$ | $V_O$=−1.0V | 1.5 | | | mA |
| Output Current "L" Level | $I_{OL2}$ | $V_O$=−14V | 2.0 | | | mA |
| Output Leakage Current | $I_{LOL2}$ | $V_O$=$V_{DD}$ | | | 30 | μA |
| Output Leakage Current | $I_{LOH2}$ | $V_O$=GND | | | 30 | μA |
| CP1, CP2 Output Terminal | | | | | | |
| Output Current "H" Level | $I_{OH3}$ | $V_O$=−1.0V | 10 | | | mA |
| Output Current "L" Level | $I_{OL3}$ | $V_O$=−14V | 10 | | | mA |
| Output Leakage Current | $I_{LOL3}$ | $V_O$=$V_{DD}$ | | | 30 | μA |
| Output Leakage Current | $I_{LOH3}$ | $V_O$=GND | | | 30 | μA |
| $V_{GG}$ Output Terminal* | | | | | | |
| Output Voltage | $V_{GG\ OUT}$ | | | −14.0 | | V |

* This terminal outputs $V_{GG}$ voltage particularly suitable for the BBD's manufactured by Matsushita Electronics Corporation. The voltage is not necessarily suitable for other manufacturers' products.
The $V_{GG\ OUT}$ changes depending on $V_{DD}$. The relationship between $V_{GG\ OUT}$ and $V_{DD}$ is as follows:

$$V_{GG\ OUT} \approx \frac{14}{15} V_{DD}$$

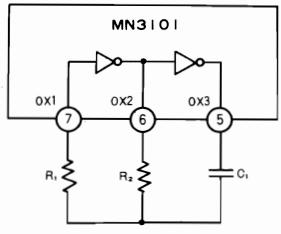
## Terminal Assignments




(Top View)

| Pin No. | Symbol | I/Ō | Functions | |
|---|---|---|---|---|
| 1 | GND | Supply | Grounding | |
| 2 | CP1 | Ō | Outputs 1/2 duty cycle clock pulse at frequency 1/2 of an oscillation frequency, having an opposite phase relationship with respect to CP2. | |
| 3 | $V_{DD}$ | Supply | −15V supply voltage input. | |
| 4 | CP2 | Ō | Outputs clock pulse having an opposite phase relationship with respect to CP1. | |
| 5 | ŌX3 | Ō | Internal Oscillation: | External Oscillation: |
| 6 | ŌX2 | Ō | C, R network connection to the pins | An external oscillation input to OX1, |
| 7 | ŌX1 | I | (See oscillator circuit example) | with OX2 and OX3 open. |
| 8 | $V_{GG\ OUT}$ | O | −14V output (When $V_{DD}$=15V)<br>The relationship between $V_{DD}$ and $V_{GG\ OUT}$ is:<br>$V_{GG\ OUT} = \frac{14}{15} V_{DD}$ | |

## Oscillator Circuit Example

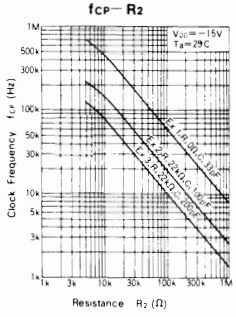



The internal oscillation circuit of the MN3101 consists of a 2-stage inverter. The oscillation frequency is established by the time constant of $C_1$ and $R_2$. The following table shows examples of $C_1$,$R_1$ and $R_2$ values. Fcp−$R_2$ characteristics example is shown in Figure 1.

### $C_1$, $R_1$ and $R_2$ Value Examples

| Example \ Constant | $R_1$ (Ω) | $R_2$ (Ω) | $C_1$ (pF) | $f_{osc}$** (kHz) | $f_{cp}$* (kHz) |
|---|---|---|---|---|---|
| Example ① | 0 | 5k~1M | 33 | 15~1500 | 7.5~750 |
| Example ② | 22k | 5k~1M | 100 | 5.2~440 | 2.6~220 |
| Example ③ | 22k | 5k~1M | 200 | 1.4~280 | 0.7~140 |

* Clock output frequency for CP1 or CP2.
** Oscillation frequency for OX1, OX2 and OX3.



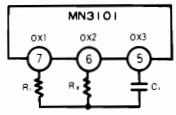




Fig 1 Clock Frequency Characteristics Example

## Maximum Clock Frequency

The maximum clock frequency is limited by device power dissipation and load capacitance. The power consumption of the device increases as the clock frequency or load capacitance is increased (See Fig. 2). Therefore, a proper clock frequency and load capacitance value must be chosen so that the maximum allowable power dissipation of 200mW for the MN3101 is not exceeded.

Fig. 3 shows the relationship between the maximum frequency and load capacitance for 150mW power dissipation. The maximum clock frequency can be increased without increasing the power consumption when a resistor is connected to each clock output terminal (See Fig. 2 and 3). The series resistor consumes a part of the power required for driving the load capacitance and help reduce the power dissipated in the device.

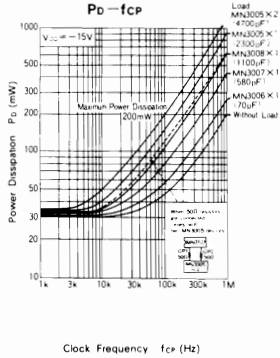



Fig. 2 Power Consumption vs Clock Frequency

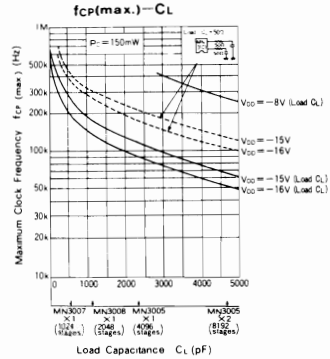
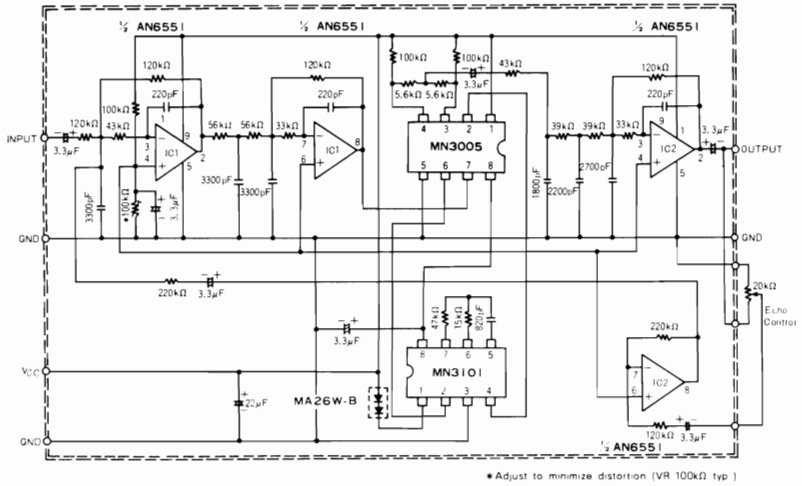
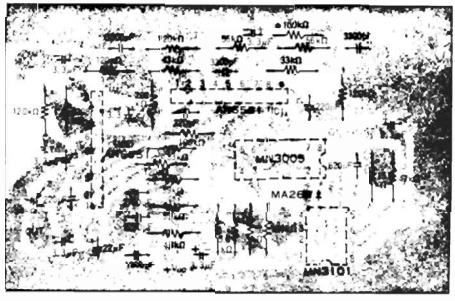

fCP(max.) — CL
PD = 150mW
VDD = −8V (Load CL)
VDD = −15V
VDD = −16V
VDD = −15V (Load CL)
VDD = −16V (Load CL)
Maximum Clock Frequency fCP (max.) (Hz)
Load Capacitance CL (pF)

Fig. 3 Maximum Clock Frequency vs Load Capacitance at 150mW Power Consumption

**Application Circuit Example 1** ——— Echo Effect Generation Circuit With The MN3005




**Printed Circuit Board Layout (actual size)**



## Quick Reference Data for The MN3005

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$ $V_{GG}$ | −15, $V_{DD}$+1 | V |
| Signal Delay Time | $t_D$ | 20.48~204.8 | msec |
| Total Harmonic Distortion | THD | 1 | % |
| Signal to Noise Ratio | S/N | 75 | dB |

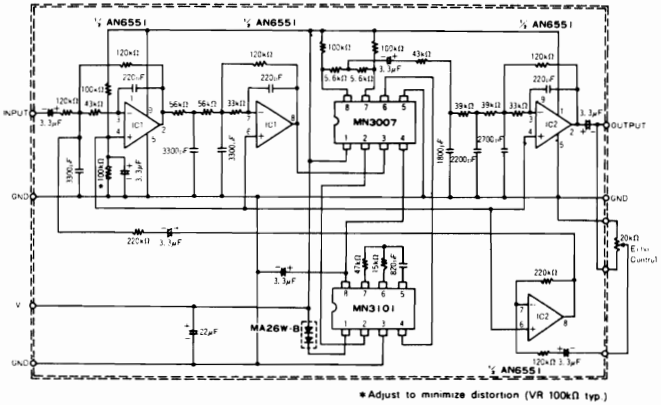
## Quick Reference Data for The AN6551

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 15 | V |
| | $V_{EE}$ | −15 | V |
| Input Bias Current | $I_B$ | 500max | nA |
| Voltage Gain | $G_V$ | 100typ | dB |
| Noise Voltage Refered to Input | $V_{NI}$ | 2.5typ | μVrms |
| Maximum Output Voltage | $V_O$(max) | ±13typ | V |
| Common-Mode Rejection Ratio | CMR | 90typ | dB |
| Supply Voltage Rejection | SVR | 30typ | μV/V |

## Electrical Characteristics of The Application Circuit Using The MN3005 ($V_{CC}$=9V, Ta=25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | | | 8 | 10 | mA |
| Total Power Consumption | Ptot | | | 70 | | mW |
| Signal Delay Time | $t_D$ | fcp=18±2kHz | 100 | 113 | 128 | msec |
| Cutoff Frequency | $f_{CO}$ | | | 2 | | kHz |
| Input signal Swing | $V_i$ | THD=2.5% | | | 500 | mVrms |
| Insertion Loss | $L_i$ | $f_i$=1kHz, $V_i$=300mV | −2 | 0 | 2 | dB |
| Total Harmonic Distortion | THD | $f_i$=1kHz, $V_i$=$V_i$(max)−6dB | | 0.5 | 1 | % |
| Output Noise Voltage | Vno | $V_i$=0V | | | 0.35 | mVrms |
| Signal to Noise Ratio | S/N | $V_S$ $V_i$(max)=500mVrms | 60 | | | dB |

## Application Circuit Example 2 —— Echo Effect Generation Circuit With The MN3007




### Printed Circuit Board Layout (actual size)

## Quick Reference Data for The MN3007

| Item | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{DD}$, $V_{GG}$ | −15, $V_{DD}$+1 | V |
| Signal Delay Time | $t_D$ | 5.12~51.2 | msec |
| Toal Harmonic Distortion | THD | 0.3 | % |
| Signal to Noise Ratio | S/N | 88 | dB |

## Electrical Characteristics of The Application Circuit Using The MN3007 ($V_{CC}$=9V, Ta=25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | | | 8 | 10 | mA |
| Total Power Consumption | Ptot | | | 70 | | mW |
| Signal Delay Time | $t_D$ | $f_{CP}$=14±2kHz | 32 | 37 | 43 | msec |
| Cutoff Frequency | $f_{CO}$ | | | 2 | | kHz |
| Input Signal Swing | $V_i$ | THD=2.5% | | | 500 | mVrms |
| Insertion Loss | $L_i$ | $f_i$=1kHz, $V_i$=300mV | −2 | 0 | 2 | dB |
| Total Harmonic Distortion | THD | $f_i$=1kHz, $V_i$=$V_i$(max)−6dB | | 0.5 | 1 | % |
| Output Noise Voltage | $V_{no}$ | $V_i$=0V | | | 0.35 | mVrms |
| Signal to Noise Ratio | S/N | $V_S$ $V_i$(max)=500mVrms | 60 | | | dB |

The SAD-512D is a general-purpose *S*ampled *A*nalog *D*elay device fabricated using N-channel silicon-gate technology in a bucket-brigade configuration to obtain flexible performance at low cost.

## KEY FEATURES

- 512-element delay
- On-chip driver requiring only single TTL-level clock input
- Clock-controlled delay: 0.2 sec to less than 200 $\mu$sec
- N-channel silicon-gate bucket-brigade technology
- Designed for self-cancellation of clocking modulation
- Wide signal-frequency range: 0 to more than 300 KHz
- Wide sampling clock frequency range: 1.5 KHz to more than 1.5 MHz
- Wide dynamic range: S/N > 70 dB
- Low distortion: less than 1%
- Single 15 volt power supply
- 8 pin mini DIP

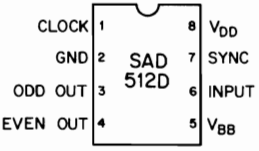



**Figure 1. Pin Configuration.**

## TYPICAL APPLICATIONS

- Voice control of tape recorders
- Control of equalization filters
- Reverberation effects in stereo equipment
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Voice scrambling systems

## DEVICE DESCRIPTION

The SAD-512D is a 512-element Bucket-Brigade Device (BBD) with internal clock drivers that require only a 5 volt (or higher) single-phase clock input.

The device has its output split into two channels to provide output over each full clock period in normal operation. The SAD-512D is manufactured using N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket-brigade charge-transfer device. It is packaged in a standard 8-lead dual-in-line package with pin configuration as shown in Fig. 1. The functional equivalent circuit is shown in Fig. 2. Several of the many applications are listed above.

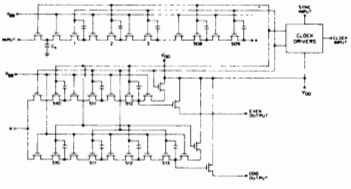


**Figure 2. Equivalent Circuit-Diagram of SAD-512D.**

## DRIVE AND VOLTAGE REQUIREMENTS

Normal voltage levels and limits are given in the tabular specifications. Clock input is a rectangular wave which drives the on-chip clock drivers. The magnitude of the clock may be any positive pulse voltage from 5 volts to $V_{DD}$. The phase relationships of clock input, sync input (when used) and output waveforms are shown in Fig. 3. For convenience, $V_{BB}$ may be biased to the same potential as $V_{DD}$. However, for optimum performance, it is recommended that $V_{BB}$ be adjusted approximately one volt lower than $V_{DD}$.

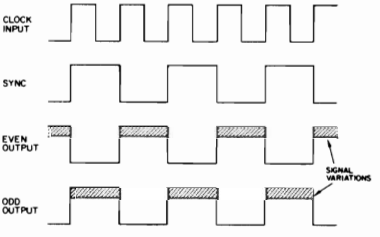



**Figure 3. SAD-512D Clock Waveforms.**

If the sync input is unused pin 7 should be connected to ground. If either output is unused it should be connected to $V_{DD}$.

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 $f_s$). Further, to recover a smooth delayed analog output a post filter having steep cutoff (e.g., 36 dB per octave or more) is desirable.

## PERFORMANCE

Typical performance of the device is shown in the specifications and in the curves of Figs. 5-8. These data were obtained with the test configuration of Fig. 4. Internal dispersion becomes the limiting factor for sampling clock frequencies above 1.5 MHz.

Figures 5 and 6 indicate the linearity and show the rapid increase in distortion as the input level is increased toward

saturation. For inputs less than approximately 500 millivolts rms the distortion is less than one percent. Between this point and the noise floor there is approximately 70 dB of dynamic range. This dynamic range assumes a 20 KHz audio filter and a sample rate of 100 KHz or faster. With a 20 KHz filter and 50 KHz sample rate the dynamic range is 63 dB. Broad-band dynamic range is better than 55 dB for all sample rates.

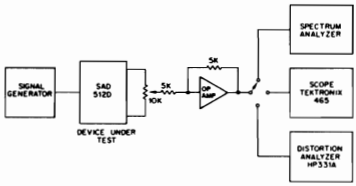



**Figure 4. Test Set-up Used to Obtain the Data of Figures 5, 6, and 7.**

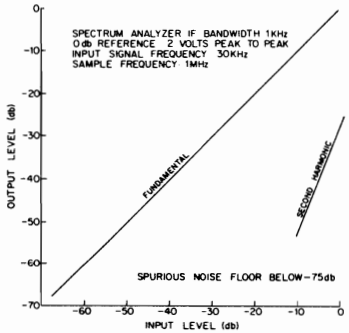



**Figure 5. SAD-512D Transfer Characteristic.**

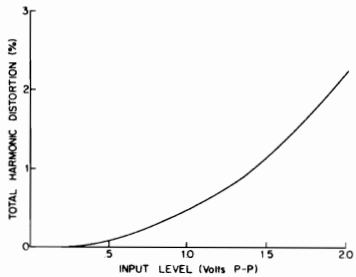



**Figure 6. SAD-512D Distortion vs. Input Level.**

Figure 7 shows the loading effect of the output terminating resistor. The data indicates the output source followers have approximately 4000 ohms internal impedance, For this test each output was connected through a terminating resistor to ground, thus preventing any interaction between the two output followers.

Figure 8 shows the frequency response of the device when terminated as shown. The dotted lines indicate the range of variation from device to device.

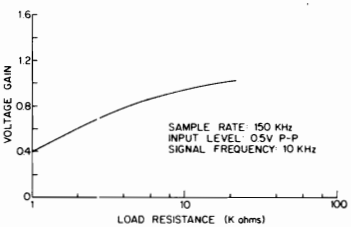



**Figure 7. Dependence of Gain on Load Resistance.**

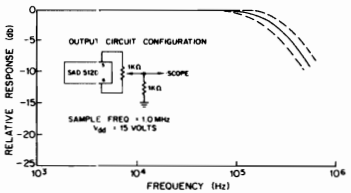



**Figure 8. Frequency Response Showing Typical Variation Device to Device.**

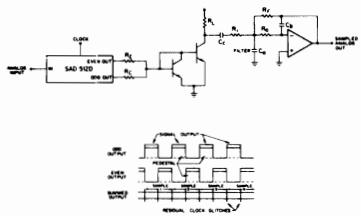



**Figure 9. Normal Operating Configuration.**

## CIRCUIT CONFIGURATION

The normal operating configuration is shown in Fig. 9. The odd and even outputs are summed to provide continuous output and cancellation of the clock waveforms. The even output contains the same information as the odd output, only delayed for one-half clock period, or a total of 513 elements of delay. The data input, odd and even outputs, and summed output are also shown in Fig. 9.

A sync input is included on the device and the waveform is shown in Fig. 3. This input allows synchronized operation of multiple devices in either serial or parallel configuration when the same sync pulse is applied to each individual SAD-512D. If the devices are used individually the sync input (pin 7) should be grounded.

## PERFORMANCE CONSIDERATIONS

The SAD-512D, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or correction, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency.

The analog input should be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable — to a limit more nearly 0.3 $f_{sample}$. The reason for this requirement is that all input components become modulated by the sampling frequency to generate ($f_s - f_{in}$) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear an equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components.

The output should be filtered because even after full-wave combination, the output is only stepwise continuous. Clocking steps and transient "glitches" appear at the times of clock transitions. The high frequencies contained in the abrupt changes and in the clocking glitches are all extraneous and for best performance should be removed by a filter with cutoff at approximately $f_{sample}/2$ or less and rolloff of as much as 36 dB/octave or more. Also, overload should be avoided because increased signal amplitude near overload gives rise to rapidly increasing high-order intermodulation products which lie within the useful pass band and which thus are not normally reducible by output filtering.

For optimized performance, care should be given to layout and design as well as to the filtering requirements. Ground planes are required on circuit boards to reduce cross-talk, and high-quality summing operational amplifiers are required to obtain maximum cancellation of clock pedestals and glitches.

For many applications, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved. For such relaxed requirements, a simple output circuit such as that shown in Fig. 10 is often useful.

## DEVICE CHARACTERISTICS AND OPERATING PARAMETERS

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|---|
| Clock Voltage[1] | $V_c$ | 5 | | $V_{DD}$ | Volts |
| Drain Supply Voltage[1] | $V_{DD}$ | 10 | 15 | 17 | Volts |
| Control Bias Voltage[1] | $V_{BB}$ | | $V_{DD}-1$ | $V_{DD}$ | Volts |
| Sampling Frequency (½ External Clock Frequency) | $f_s$ | 0.0015 | — | 1.5 | MHz |
| Clock Pulse Width | $t_{cp}$ | 200 | $t_c/2$ | $t_c-200$ | ns |
| Signal Frequency Bandwidth (3db point) | | See Fig. 8 | 300 | | KHz |
| Signal to Noise | | See Fig. 5 | | | |
| Distortion | | See Fig. 6 | | | |
| Gain[2] | | | .8 | | |
| Video Input Capacitance | $C_{in}$ | | 15 | | pf |
| Video Input Shunt Resistance[3] | $R_{in}$ | 300 | | | Kohms |
| Output Resistance | $R_o$ | See Fig. 7 | | | |
| Optimum Signal Input Bias[4] | | | 4.2 | | Volts |
| Maximum Input Signal Amplitude | | 1 | 2 | | Volts p-p |
| Sync Pulse Amplitude | | 5 | | $V_{DD}$ | Volts |
| Clock Input Capacitance | $C_c$ | | 8 | | pf |

*Notes:*

1. *All voltages measured with respect to GND (pin 2).*
2. *The value of gain depends on the output termination resistance. See Fig. 7.*
3. *Effective a-c shunt resistance measured at 1 MHz sample rate.*
4. *The input bias voltage varies slightly with the magnitude of the clock voltage (and $V_{dd}$) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 15-volt clocks.*

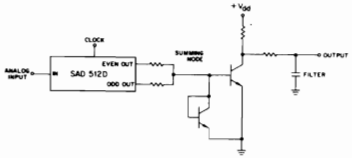



**Figure 10. Simple Output Summing Amplifier.**

## EVALUATION CIRCUIT SC-512D

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the required filters, operational amplifiers, and ground plane. The schematic is shown in Fig. 11. The board provides a variable oscillator for sample frequencies from 20 KHz to 200 KHz. The output filter amplifier is designed as a two-pole, maximally flat filter with a cutoff frequency of 25 KHz. Change in cutoff frequency requires component changes. The balance control permits equalization of differences in source follower outputs.

The SC-512D board is designed to handle a wide range of bandwidths and clock rates; as a consequence anti-aliasing input filters should be externally provided to limit the input bandwidth to less than $f_{sample}/2$.

## ABSOLUTE MAXIMUM VOLTAGES

| TERMINAL | LIMITS | UNITS |
|---|---|---|
| Any terminal (with respect to GND) | +20 to -0.4 | Volts |

## CAUTION

Static discharge to any lead of this device may cause permanent damage. Store with shorting clip or inserted in conductive foam. Use grounded soldering irons, tools, and personnel when handling devices. Avoid synthetic fabric smocks and gloves. It is recommended that the device be inserted into socket before applying power. Power supplies should not exhibit turn-on or turn-off spikes.

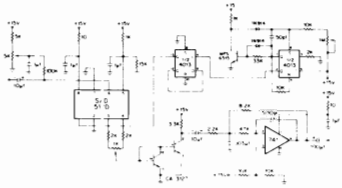


**Figure 11. SC-512D Schematic Diagram.**

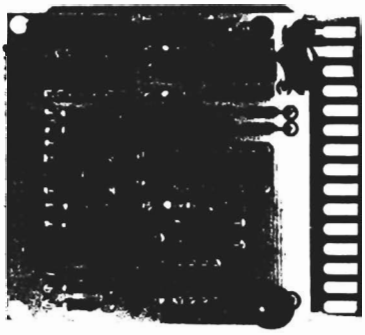


**Figure 12. SC-512D Evaluation Circuit with SAD 512D Device.**

87270

# EG&G RETICON

## SAD-1024 DUAL ANALOG DELAY LINE
## SAD-512 ANALOG DELAY LINE

The **SAD-1024** is a general-purpose **S**ampled **A**nalog **D**elay device fabricated using N-channel silicon-gate technology in a bucket-brigade configuration to obtain flexible performance at low cost.

**Two independent 512-stage delay sections.**
**Clock-controlled delay: 0.34 sec to less than 340$\mu$sec.**
**N-channel silicon-gate bucket-brigade technology.**
**Designed for self-cancellation of clocking modulation.**
**Wide signal-frequency range: 0 to more than 200KHz.**
**Wide sampling clock frequency range: 1.5KHz to more than 1.5MHz.**
**Wide dynamic range: S/N > 70db.**
**Low distortion: less than 1%.**
**Low noise**
**Single 15 volt power supply.**

**Voice control of tape recorders.**
**Variable signal control of amplitude or of equalization filters.**
**Reverberation effects in stereo equipment.**
**Tremolo, vibrato, or chorus effects in electronic musical instruments.**
**Variable or fixed delay of analog signals.**
**Time compression of telephone conversations or other analog signals.**
**Voice scrambling systems.**

## DEVICE DESCRIPTION

The SAD-1024 is a dual 512-stage Bucket-Brigade Device (BBD). Each 512-stage section is independent as to input, output, and clock. The sections may be used independently, may be multiplexed to give an increased effective sample rate, may be connected in series to give increased delay at a fixed sample rate, or may be operated in a differential mode for reduced even-harmonic distortion and reduced clocking noise. Each section has its output split into two channels so that in normal operation output is provided over each full clock period. The SAD-1024 is manufactured using N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket brigade charge-transfer device. It is packaged in a standard 16-lead dual-in-line package with pin configuration as shown in Figure 1. Only $V_{dd}$ and GND are common to the two separate delay sections. Figure 2 shows the functional equivalent circuit diagram. Some of the many applications are listed above.

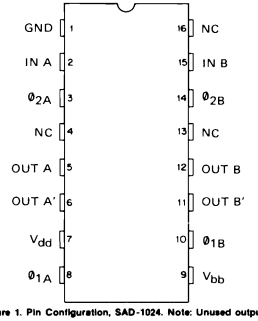



**Figure 1. Pin Configuration, SAD-1024. Note: Unused outputs should be connected to $V_{dd}$; all other unused pins should be connected to GND (pin 1), including those marked N.C.**

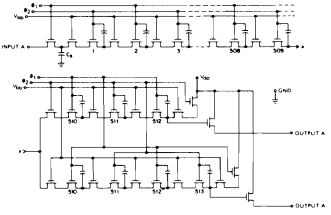


**Figure 2. Equivalent Circuit Diagram of either 512-Stage Section of the SAD-1024.**

Normal voltage levels and limits are given in the tabular specifications. Clock inputs are two-phase square waves ($Ø_2$ is the complement of $Ø_1$) which swing between ground and $V_{dd}$. For convenience, $V_{bb}$ may be biased to the same potential as $V_{dd}$. However, for optimum performance, it is recommended that $V_{bb}$ be adjusted approximately one volt lower than $V_{dd}$, and that the clock amplitude equal $V_{dd}$. Unused outputs only should be connected to $V_{dd}$; other unused terminals (including those marked N.C.) should be connected to ground.

The input analog signal is connected through the first MOS transistor to the input storage capacitor while $Ø_1$ is high; the charge is then transmitted to the next bucket-brigade stage when $Ø_1$ is low, $Ø_2$ high. Thus the signal samples are those values in existence at the positive-to-negative transitions of $Ø_1$ and the input sample rate $f_S$ is the same as $f_{Ø_1}$.

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TELEPHONE: (408) 738-4266 • TWX 910-339-9343

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 $f_S$). Further, to recover a smooth delayed analog output a post filter having steep cutoff (e.g., 36 db per octave) is desirable.

## PERFORMANCE

Typical performance of the device is shown in the specifications and in the curves of Figures 4-7. These data were obtained with the test configuration of Figure 3. Internal dispersion becomes the limiting factor for sampling clock frequencies above 1.5MHz.

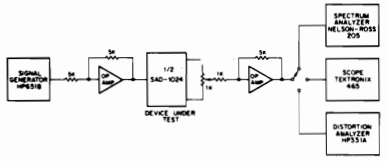


**Figure 3. Test Set-up used to obtain the data of Figures 4, 5 and 6.**

Figures 4 and 5 indicate the linearity and show the rapid increase in distortion as the input level is increased toward saturation. For inputs less than approximately 500 millivolts rms the distortion is less than one percent. Between this point and the noise floor there is approximately 70 db of dynamic range.

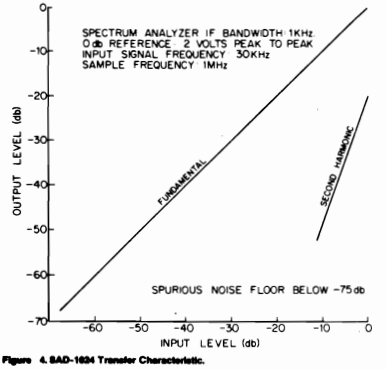


**Figure 4. SAD-1024 Transfer Characteristic.**

Figure 6 shows the loading effect of the output terminating resistor. The data indicate the output source followers have approximately 400 ohms internal impedance. For this test each output was connected through a terminating resistor to ground, thus isolating any interaction between the two output followers.

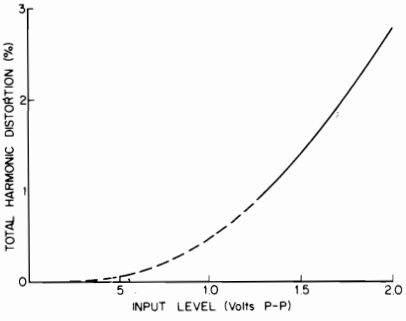


**Figure 5. SAD-1024 Distortion vs. Input Level.**

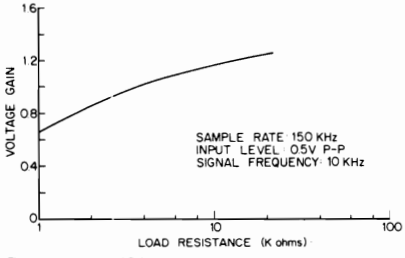


**Figure 6. Dependence of Gain on Load Resistance.**

Figure 7 shows the frequency response of the device when terminated as shown. The dotted lines indicate the range of variation from device to device.

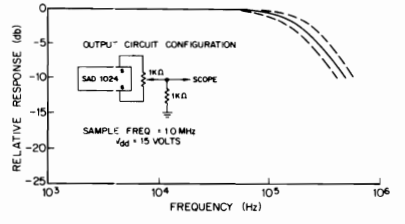


**Figure 7. Frequency Response showing Typical Variation Device to Device.**

## CIRCUIT CONFIGURATIONS

Each SAD-1024 consists of two 512-element delay sections electrically independent except for common grounds and power supplies. The sections may be used in series, in parallel multiplex, in a differential mode, or as completely separate de-

vices. But note that for a given system sample rate, the parallel or differential configuration may be preferable to the series configuration. A number of possible arrangements using one or two devices are described in the following sections.

## 1. Normal single-section configuration

In this configuration, the A and B sections are independent except for common power-supply connections. Different input signals and different clocks are permissible. A and A' outputs should be summed externally as in Figure 8. The B and B' outputs should be similarly summed for the second channel. Delay is 512 clock half periods between the input cutoff at the falling edge of $\phi_{1A}$ to the end of the output at video A (when $\phi_{1A}$ likewise falls). Output A' then appears (with the value previously at Output A) and exists for the next or 513th clock half period. A clock half period is the time duration between successive clock transitions, or one half of a full square-wave cycle. The A section is used for illustration only; the B section performance is completely similar but independent from A.

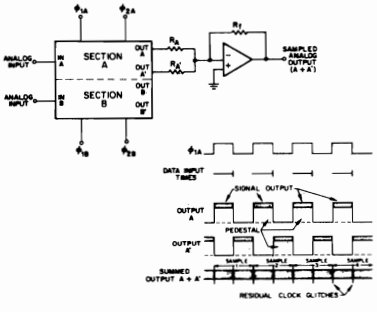


**Figure 8. Single-Section Operation. Connect unused outputs to $V_{dd}$ and all other unused pins to ground.**

## 2. Serial configuration

This configuration doubles the permissible delay time for a given sample rate. It is generally preferred when longer delays are required than can be obtained from a single section.

In the serial configuration, output from channel A is slightly attenuated to restore the level to equal that originally input to A, and this modified signal then connected to input B, as in Figure 9. $\phi_{1A}$ and $\phi_{1B}$ are connected together as are $\phi_{2A}$ and $\phi_{2B}$. Under these conditions the input to B is that corresponding to output A. Output A' need not be used except to reduce transients in the output amplifier. It is also possible to obtain 513 clock half-periods of delay from section A by using output A' to connect to input B and reversing the clocks to B. Unused outputs should be terminated to $V_{dd}$.

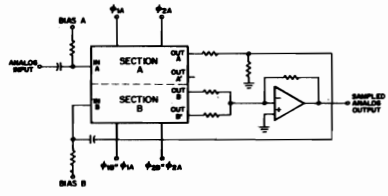


**Figure 9. Serial Connection of Delay Sections. Waveforms are entirely similar to those for single-section operation (Figure 8). Connect unused outputs to $V_{dd}$.**

For this configuration note that there is only one sample per clock period, but two clock "glitches" per sample in the output. The Nyquist frequency is $f_N = f_{sample}/2 = f_{clock}/2$.

## 3. Parallel-multiplex operation

This configuration doubles the number of samples for the same delay or doubles the delay for the same sample rate, when compared to single-section performance. When sample rate is held constant and delay doubled, the individual sections operate at one-half the system rate, so that superior performance is possible. In the parallel multiplex operation, the inputs are paralleled, but the clocks to section B are reversed from those to section A as in Figure 10. Now, on the posi-

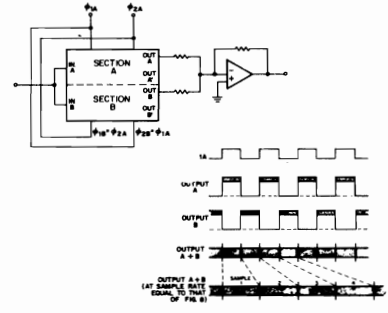


**Figure 10. Parallel-Multiplex Operation. Connect unused outputs to $V_{dd}$.**

tive portion of $\phi_{1A}$, data is input to section A, to be held and propagated down the bucket brigade at the value present when $\phi_{1A}$ falls. Data to section B is input during the positive portion of $\phi_{1B}$, which is the same as $\phi_{2A}$, so that data is alternately sampled into section A and section B, one sample per half-period of the clock. At the outputs we now sum either outputs A and B (for 512 clock half-periods of delay) or outputs A' and B' (for 513 clock half-periods of delay), but now there are two samples overall per clock period instead of only one. Thus the Nyquist frequency overall is $F_N = f_{sample}/2 = f_{clock}$, or double that for the single section or serial sections operating at the same clock rate. One could thus halve the clock rate to keep the overall sampling rate and Nyquist frequency the same as for the single or serialed sections, but delay is twice that for a single section (equal to that for the serialed sections.) Multiplex operation is generally preferable only when operating at high sample frequencies, as a means of reducing individual section rates. For sample rates of 200 KHz or below, other limitations generally favor serial operation. As before, unused outputs should be connected to $V_{dd}$ and other unused pins grounded.

### 4. Differential Operation.

In this configuration, more effective cancellation of clocking glitches is possible, because the *same* clock transitions are combined differentially and even-harmonic distortion cancels. The arrangement is as in Figure 11. Operation is similar to that for single-channel operation except for the differential cancellation of the output pedestals and clocking glitches, and cancellation of even harmonics, as in push-pull operation. It should be obvious that two devices could be combined in parallel-multiplex, with each device differentially connected, to give the benefits of a Nyquist frequency equal to the clock frequency, as well as the benefits of differential operation.

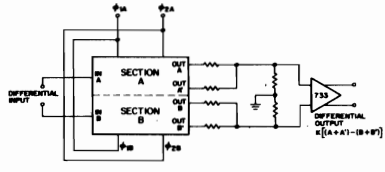


Figure 11. Differential Operation.

### 5. Multiple-device Operation.

Extension of any of the above methods of operation to multiple devices is possible. Serial operation is restricted by the requirement of gain restoration between sections, by increased dispersion as the number of BBD cells increases, and by all the switching noise of single devices. Note that the SAD-1024 itself exhibits slightly more than unity gain, so that direct serial connection through a resistance network is possible.

Additional units may be multiplexed in the parallel-multiplex configuration by shifting the phase of the clock to successive devices by $\pi/N$ radians where N is the number of devices. Thus in the case of two devices, for example, device #2 has its clocks shifted by $\pi/2$ radians or 90° from those of device #1.

## PERFORMANCE CONSIDERATIONS

The SAD-1024, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or correction, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency. Also, increased signal amplitude near overload gives rise to rapidly increasing intermodulation products which lie within the useful passband and which thus are not normally reducible by filtering. In the first place, the analog input must be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable—to a limit more nearly 0.3 $f_{sample}$. The reason for this requirement is that all input components become modulated by the sampling frequency to generate ($f_s$-$f_{in}$) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear an equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components. In the second place, even after combination as indicated, the output is only stepwise continuous, and clocking "glitches" appear at the times of clock transitions. The high frequencies contained in the abrupt changes and in the clocking glitches are all extraneous and for best performance should be removed by a filter with cut-off at approximately $f_{sample}/2$ or less and rolloff of as much as 36 db/octave or more.

For optimized performance, care should be given to layout and design as well as to the filtering requirements. Ground planes are required on circuit boards to reduce crosstalk, and high-quality summing operational amplifiers are required to obtain maximum cancellation of clock pedestals and glitches.

For many applications, however, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved. For such relaxed requirements, a simple output circuit such as that shown in Figure 12 is often useful.

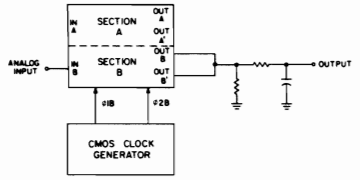


Figure 12a. Simple Output Summing Circuit. Connect unused outputs to $V_{dd}$ and all other unused pins to ground.

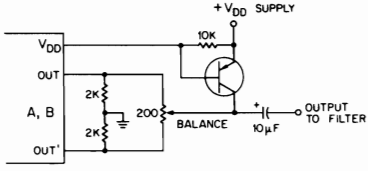


Figure 12b. Feedback Impedance Convert Circuit. Provides improved frequency response and low output impedance. Connect unused outputs to $V_{dd}$ and all other unused pins to ground.

Figure 13. Photograph of SC-1024A Evaluation Board.

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the desired filters, clock control, and ground plane. External balanced + and − power supply (nominally ±15 volts) and TTL clock drive is required. Figure 13 is a photograph of the board and Figure 14 is its schematic diagram. Note that the board is arranged such that the two halves of the SAD-1024 may be operated independently, or in series as desired. The separate connection also permits parallel multiplex or differential operation; the series connection is useful for longer delay.

Each output filter amplifier is nominally designed as a two-pole maximally flat filter with cutoff frequency of approximately 20KHz. They follow standard active two-pole filter design, with the source impedance of the SAD-1024 and the balance arrangements taken into account. Change of cutoff frequency requires component changes. For the separate configuration, each section of the SAD-1024 is provided with its own two-pole filter; for the series configuration, the filters are cascaded to improve the out-of-band attenuation. The SAD-1024 provides output from terminal A (or B) during the period $Ø_1$ is high and output from A' (or B') when $Ø_2$ is high. These outputs are summed at the balance potentiometer whose adjustment permits equalization for slight differences in the source-follower outputs from the SAD-1024. The board SC-1024A is designed to handle a wide range of bandwidths and clock rates; as a consequence no attempt has been made to provide band limiting at the input. Anti-aliasing filters should be provided externally if the input is not otherwise limited to a bandwidth less than $f_{sample}/2$.

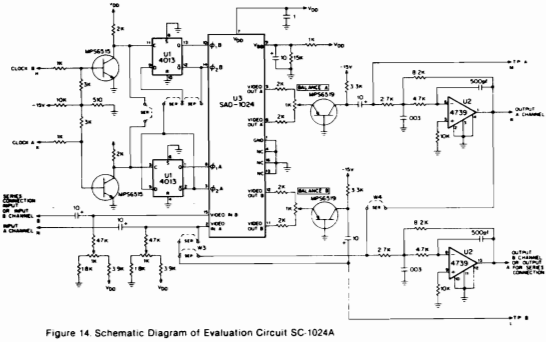

Figure 14. Schematic Diagram of Evaluation Circuit SC-1024A

## DEVICE CHARACTERISTICS AND OPERATING PARAMETERS

| PARAMETER | SYMBOL | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Clock Voltage[1] | $\phi_1$, $\phi_2$ | 10 | 15 | 17 | Volts |
| Drain Supply Voltage[1] | $V_{dd}$ | 10 | 15 | 17 | Volts |
| Bias Voltage[1] | $V_{bb}$ | | $V_{dd}$-1 | $V_{dd}$ | Volts |
| Sampling Freq. | $f\phi_1$, $f\phi_2$ | 0.0015 | — | 1.5 | MHz |
| Clock Rise Time | $t_{cr}$ | | 30 | | nsec |
| Clock Fall Time | $t_{cf}$ | | 50 | | nsec |
| Clock Line Cap | $C_c$ | | 110 | | pf |
| Signal Freq. Bandwidth (3db point) | | See Fig. 7 | 200 | | KHz |
| Signal to Noise | | See Fig. 4 | | | |
| Distortion | | See Fig. 5 | | | |
| Gain[2] | | | 1.2 | | |
| Input Capacitance | $C_{in}$ | | 7 | | pf |
| Input Shunt Resistance[3] | $R_{in}$ | | | 200 | Kohms |
| Output Resistance | $R_o$ | See Fig. 6 | | | |
| Optimum Input Bias[4] | | | +6 | | Volts |
| Maximum Input Signal Amplitude | | 1 | 2 | | Volts p-p |
| Average Temp. Coefficient of Gain[5] | | | -.01 | | db/°C |
| Average Temp. Coefficient of Optimum Input Bias[6] | | | .8 | | mv/°C |

## ABSOLUTE MAXIMUM VOLTAGES

| TERMINAL | LIMITS | UNITS |
|---|---|---|
| Any terminal[1] | +20 to -0.4 | Volts |

**Notes:**

1. All voltages measured with respect to GND (pin 1).
2. The value of gain depends on the output termination resistance. See Figure 6.
3. Effective a-c shunt resistance measured at 1MHz.
4. The input bias voltage varies slightly with the magnitude of the clock voltage (and $V_{\phi\phi}$) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 15 volt clocks.
5. The device may be operated at clock voltages down to 5 volts (to facilitate use in battery operated portable equipment) but with reduced input bias and reduced input signal amplitude.
6. Measured at sample frequency of 10KHz, audio input of 1V p-p at 1KHz in SC-1024A circuit for temperature range of 0° to 70°C.

**WARNING:** Observe MOS Handling and Operating Procedures. Maximum rated supply voltages must not be exceeded. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

## SAD-512 SINGLE 512-STAGE ANALOG DELAY LINE

The SAD-512 is identical to one 512-stage section of the SAD-1024; all of the specifications and characteristics of the latter device apply equally to the SAD-512. Figure 15 shows the pin configuration of the SAD-512. Note that pin assignments are identical to those for the A section of the SAD-1024. In some instances, SAD-1024 devices having an inoperative B section may be used to make SAD-512 devices. It is, therefore, essential that unused pins 10, 14, and 15 be connected to ground, and that pins 11 and 12 be connected to $V_{dd}$.

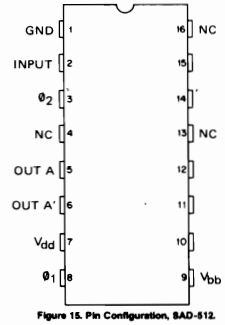


**Figure 15. Pin Configuration, SAD-512.**

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08300

The SAD-4096 is a general purpose 4096-bucket (2048-sample) n-channel bucket-brigade audio delay line useful in applications where relatively long delay is desired, coupled with high performance. The signal is sampled at the clock rate, but the samples retain their analog values. Simple filtering applied at the output smooths the stairstep of samples to recover the analog wave form.

The delay is controlled by the clock frequency according to the relation $T_D = 2048/f_c$, so that a clock or sample rate of 40 KHz, for example, the delay is 51.2 milliseconds.

Key Features

- 2048 samples of audio signal delay
- Wide dynamic range: S/N 70 db (unweighted)
- Clock-Controlled Variable delay
- Sample rates from 8 KHz to 1 MHz
- Delays from 2 msec to 250 msec
- On-chip buffers provide full-wave output

Typical Applications

- Reverberation effects
- Sound effects
- Data buffering
- Speech scramblers

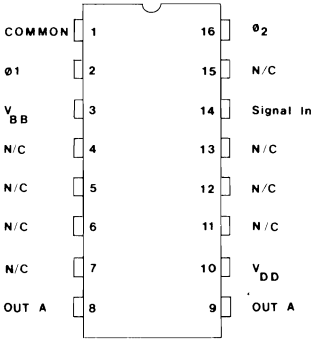



Figure 1. Pin Configuration for SAD-4096 18317

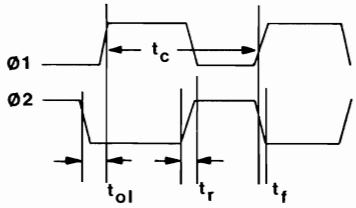
## Absolute Maximun Ratings

| | |
|---|---|
| Voltage on any pin to common (pin 1) | -0.5 to +18 volts dc or peak |
| Output Current | 5 milliamperes |
| Temperature (operating) | $0^{o}$ to $70^{o}$ C |
| Temperature (storage) | $-55^{o}$ to $125^{o}$ C |

Note: Long delays are limited by leakage to approximately o.25 second, at $25^{o}$ C at a clock rate of 8 KHz. At $70^{o}$C, the minimum sample rate rises to more than 250 KHz.

## Drive and Voltage Requirements

Normal voltage levels and linits are given in the specifications, Table I. The clock inputs are normally complementary square waves. The timing relationships are noncritical, so long as the crossing level is below the top quarter of the wave.




| | Max | Typ | Min | Units |
|---|---|---|---|---|
| $t_{ol}$ | $\frac{t_c}{2}$ - - 50 | 50 | 0 | nsec |
| $t_r$ | | 50 | 10 | nsec |
| $t_f$ | | 50 | 10 | nsec |

Figure 2. SAD-4096 Clock Timing Requirements



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TABLE I

SAD-4096 Electrical Specifications (25°C)

| Symbol | Function | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| $V_{DD}$ | Output Supply | 8 | 12-15 | 18 | Volts dc |
| $V_{BB}$ | CTD Interstage Bias Voltage | 8 | $V_{\emptyset H}$-1 | 12 | Volts dc |
| $V_{\emptyset 1L}$, $V_{\emptyset 2L}$, | CTD Clock Amplitude | -0.3 | 0 | 0.5 | Volts p |
| $V_{\emptyset_1 H}$, $V_{\emptyset_2 H}$, | | 8(1) | 12-15 | 18 | Volts p |
| $V_{IB}$ | Input Bias | 0.3 | 3(2) | 6 | Volts dc |
| Vin | ($V_{bb}$ = 11.5 volts) | | 2 | | Volts p-p |
| C$\emptyset$ | Clock Line Capacitance | | 1000 | | pf |
| $C_{in}$ | Input Capacitance | | | 2 | pf |
| $f_c$ | Clock or sample rate | 8 | 100 | 1000 | KHz |

Footnotes for Table I

(1) The device is operable to clock and supply voltages as low as 5 volts, but at substantially reduced signal levels.

(2) Input bias is dependent on the particular values of $V_{BB}$, $V_{\emptyset}$ and $V_{DD}$, so that adjustment provision should be made to fit the circumstances used.

(3) WARNING: Observe MOS Handling and Operating Procedures. Maximum rated supply voltages must not be exceeded. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

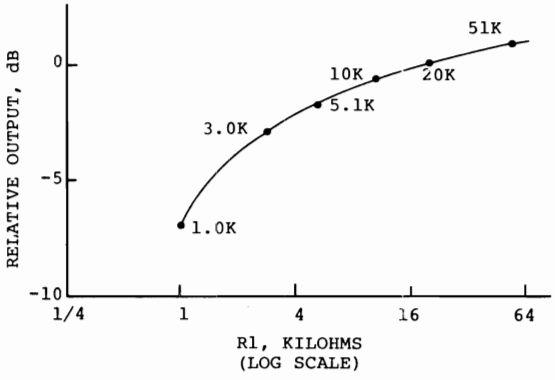



Figure 3. Effect of Load Impedance on Signal Output Level.

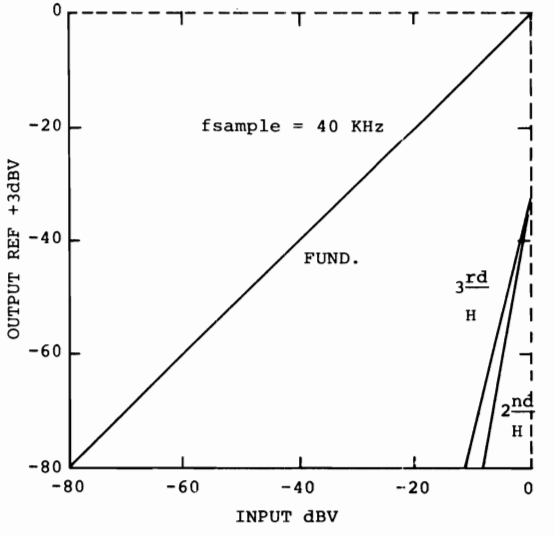



Figure 4. Signal and Harmonic Output Levels versus Input Level.

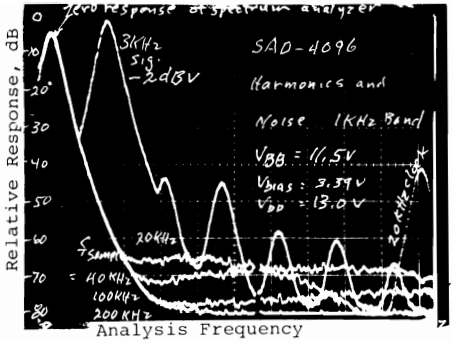



Figure 5. Spectrum Analyzer Response Showing a 3 KHz Signal and Four Traces of Noise Background at Sample Rates of 20, 40, 100 and 200 Kilohertz.

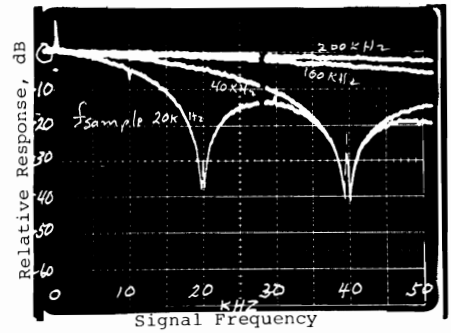
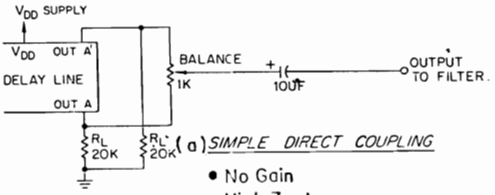


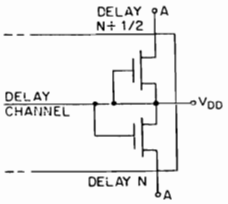

Figure 6. Frequency Response, with Output Filter, of SAD-4096 at Various Clock Rates.

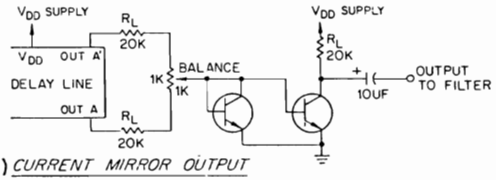
Note:
Due to the $\frac{\sin x}{x}$ sampling, the response is down 3.92 db at the Nyquist frequency.

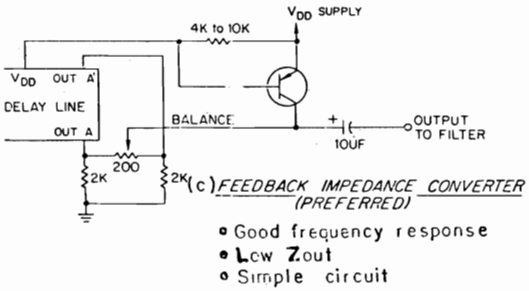
Figure 8. *SIMPLE OUTPUT CIRCUITS*




*OUTPUT CIRCUIT OF DELAY LINE*



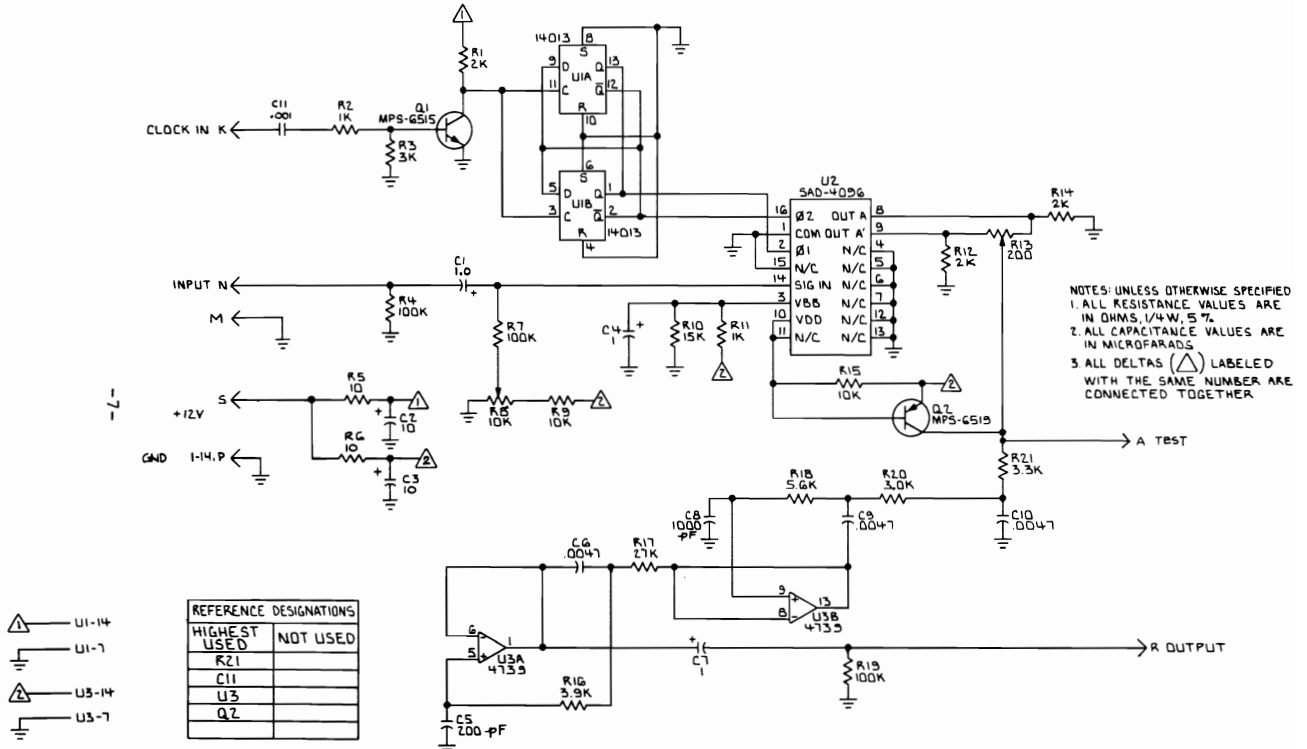



Figure 7. SC4096 Evaluation Board Schematic

CURTIS ELECTROMUSIC SPECIALTIES
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Santa Clara, CA 95051
(408) 247-8046

# CEM 3310

## Voltage Controlled Envelope Generator

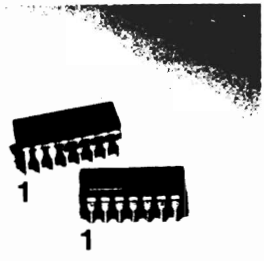
The CEM3310 is a self-contained, precision ADSR type of envelope generator intended for electronic music and other sound generation applications. Attack, decay and release times are exponentially voltage controllable over a wide range, and the sustain level is linearly voltage controllable from 0 to 100% of the peak voltage. A unique design approach allows for a 10,000 times improvement in control voltage rejection over conventional designs. In addition, much care has been given to the accuracy, repeatability and tracking of the parameters from unit to unit without external trimming. The times are to a first order determined only by the external resistor and capacitor and constant of physics, KT/q. Wide tolerance monolithic resistors are not used to set up the time constants or the control scale. Finally, all four control inputs are isolated from the rest of the circuitry so that the control pins of tracking units may be simply tied together. Although a low voltage process has been used to lower the cost and lower the leakage currents, an internal 6.5 volt Zener diode allows the chip to be powered by ± 15 volts supplies, as well as +15, -5 volt supplies.

* **Zero to -5V Varies the Times from 2mS to 20S**

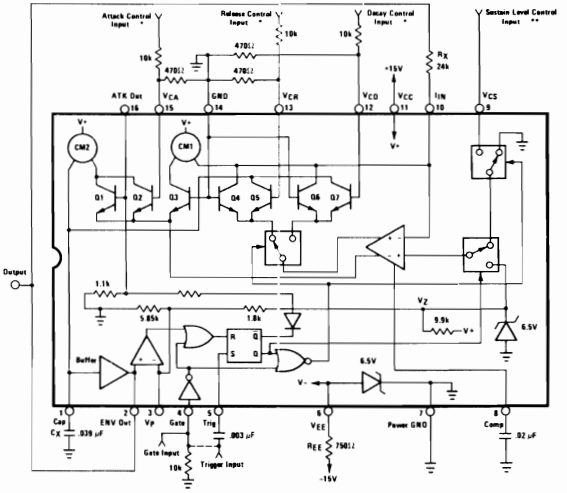
** **Zero to +5V Varies the Sustain Level from 0 to 100%**

### Features

- Low Cost
- Third Generation Design
- Large Time Control Range: 50,000 min
- Full ADSR Response
- True RC Envelope Shape
- Exceptionally Low Control Voltage Feedthrough: 90μV max
- Accurate Exponential Time Control Scales
- Isolated Control Inputs
- Good Repeatability and Tracking Between Units Without External Trim
- Independent Gate and Trigger
- ± 15 Volt Supplies




### Circuit Block and Connection Diagram



# CEM 3310

## Electrical Characteristics

| $V_{CC}$ = +15.0V $V_{EE}$ = -5.0 to -15.0V $R_X$ = 24K $T_A$ = 25°C | | | | |
|---|---|---|---|---|
| | MIN | TYP | MAX | Units |
| Time Control Range | 50,000:1 | 250,000:1 | – | |
| Attack Asymtote Voltage ($V_Z$) | 6.1 | 6.5 | 6.9 | V |
| Attack Peak Voltage ($V_p$) | 4.7 | 5.0 | 5.3 | V |
| Attack Peak to Asymptote Tracking | – | 1.5 | 4 | % |
| Control Scale Sensitivity | 58.5 | 60 | 61.5 | mV/Decade |
| Temperature Coefficient of Control Scale | +3,000 | +3,300 | +3,600 | ppm |
| ATK, DCY, RLS Scale Tracking | -300 | 0 | +300 | μV/Decade |
| Exponential Full Scale Control Accuracy[1] | | | | |
| 50nA < $I_O$ < 50 μA | – | 0.3 | 1.5 | % |
| 2nA < $I_O$ < 200 μA | – | 2 | 10 | % |
| Attack C.V. Feedthrough[2] | – | 6 | 90 | μV |
| Decay C.V. Feedthrough[2] | | NONE | | |
| Release C.V. Feedthrough[2] | | NONE | | |
| Sustain Final Voltage Error ($V_O$-$V_{CS}$) | -3 | +10 | +23 | mV |
| Release Final Voltage Error ($V_O$) | -3 | +10 | +23 | mV |
| RC Curve Asymptote Error[3] | | | | |
| $V_{CA,D,R}$ = 0 | – | -6 | -60 | μV |
| $V_{CA,D,R}$ = -240mV | – | -125 | -1250 | mV |
| Input Current ($I_{IN}$) to Output Current ($I_O$) Ratio, $V_{CA,D,R}$ = 0.5 | | | | |
| Charge Current (ATK) | .75 | 1 | 1.3 | |
| Discharge Curreht (DCY, RLS) | .83 | 1 | 1.2 | |
| Buffer Input Current ($I_{B2}$) | – | 0.5 | 5 | nA |
| Op Amp Input Current ($I_{B1}$) | 150 | 400 | 800 | nA |
| Gate Threshold | 2.0 | 2.3 | 2.6 | V |
| Gate Input Current | 5 | 25 | 100 | μA |
| Trigger Pulse Required to Trigger Envelope | +1.1 | +1.3 | +1.5 | V |
| Trigger Input Impedance | 2.4 | 3 | 4 | KΩ |
| Time Control Input Current | 0.5 | – | 2500 | nA |
| Sustain Control Input Current | 150 | 400 | 800 | nA |
| Attack Output Signal | -4 | -8 | -12 | V |
| Output Current Sink Capability | 420 | 560 | 700 | μA |
| Buffer Output Impedance | 100 | 200 | 350 | Ω |
| Positive Supply Voltage Range | +12.5 | – | +18 | V |
| Negative Supply Voltage Range[4] | -4.5 | – | -18 | V |
| Supply Current | 5.6 | 7.5 | 9.4 | mA |

**Note 1**: Scale factor determined at mid-range. Spec represents total deviation from ideal at range extremities.

**Note 2**: Output is at either sustain final voltage or release final voltage. $V_{CA,D,R}$ varies 0 to -240mV.

**Note 3**: Spec represents the difference between the actual final voltages (attack asymptote voltage, sustain final voltage, and release final voltage in the case of attack, decay, and release respectively) and the apparent voltage to which the output seems to be approaching asymptotically.

**Note 4**: Current limiting resistor required when $V_{EE}$ > -6.0 volts.

**Note 5**: Spec also represents time constant variation between units for $V_{CA,D,R}$ = 0.

## Application Hints

### Supply

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% zener diode has been provided to allow the chip to run off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 6). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 6 and the supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2)/.010.$$

The circuit was designed for a positive supply of +15 volts. Voltages other than +15 volts will cause the peak threshold voltage to be either at a minimum of .33$V_{CC}$ or at a maximum of 5.5 volts.

### Gate and Trigger Inputs

The gate input is referenced to ground and therefore will accept any ground referenced TTL or CMOS logic level up to +18 volts. If the gate pin is left floating, it will be interpreted as a high level. The trigger input is referenced to the $V_{EE}$ pin (pin 6) and therefore, a ground referenced trigger pulse should be capacitively coupled to the trigger input pin (pin 5).

### Input Control Voltages

As the scale sensitivity on the three time control inputs is 60mV/decade, attenuation of the incoming control voltages will in most cases be required. Four decades of control requires only a 240mV voltage excursion. The more negative the voltages the longer the times. For best scale accuracy at the shortest times, the impedance at the time control pins should be kept low. At the shortest times (corresponding to 200 μA of peak

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage Between $V_{CC}$ and $V_{EE}$ Pins | 24V |
| Voltage Between $V_{CC}$ and Ground Pins | +18V |
| Voltage Between $V_{EE}$ and Ground Pins | -6.0V |
| Current Into $V_{EE}$ Pin | ±50mA |
| Voltage Between Control and Ground Pins | ±6.0V |
| Voltage to Gate and Trigger Input Pins | $V_{EE}$ to $V_{CC}$ |
| Storage Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -25°C to +75°C |

current), every 100Ω will cause a 1% increase in control scale error. As the times are increased, this error will decrease in direct proportion.

The voltage applied to the sustain level control input will directly determine the sustain voltage of the output envelope (minus the sustain final voltage error). Voltages greater than the threshold voltage will cause the envelope to ramp up to this higher voltage when the peak threshold is reached. The rate at which this occurs will be equal to the fastest attack rate.

Since all four control inputs are connected only to the bases of NPN transistors, the control input pins of tracking units may be simply tied together. Therefore, in the case of the time control inputs, only one attenuator network is required to control the same parameter in a multiple chip system.

### Selection of $R_X$ and $C_X$

As is shown in the envelope equations, the RC time constant of the attack, decay and release curves is given by $R_XC_X$ times the exponential multiplier, $\exp(-V_C/V_T)$. Practical circuit limitations determine $R_X$ and the multiplier, from which $C_X$ can then be calculated. The peak capacitor charging and discharging currents is given by $(V_Z/R_X)\exp(V_{CA}/V_T)$, $(V_{CS}/R_X)\exp(V_{CD}/V_T)$, and $(V_P/R_X)\exp(V_{CR}/V_T)$ for the attack, decay, and release phases respectively. For the best scale accuracy and tracking at the shortest times, these currents should be kept less than 100 μA, and in all cases they should not be allowed to exceed 300 μA. This sets the minimum value for $R_X$ at 24K. Larger values of $R_X$ will allow positive time control voltages to be used. However, as can also be seen from the envelope equations, the sustain/final voltage error, the asymptote error, and the control voltage feedthrough are all affected by $R_X$. A practical maximum of 240K is recommended for $R_X$ when the internal buffer is used and 1M if an external FET buffer is used.

### Trimming the Envelope Times

The RC time constants of the output envelope will typically track to within ± 15% from unit to unit, even at the longest time settings. If better tracking is required, the best method for trimming the time constants is to simply adjust $R_X$ with a trimming potentiometer.

### Output Drive Capability

The buffer output can sink at least 400 μA and can source up to 10mA, but with considerable degradation in performance. An output load no less than 20K to ground is recommended.

The buffer has a somewhat high output impedance. As a result of this, small steps (50mV) appear in the output waveform at the phase transitions, due to the sudden change in drive the output must provide to $R_X$. The largest step is at the beginning of the envelope and is given by $(R_O/R_X)V_Z$. It may be decreased by increasing $R_X$, lowering $R_O$, or using an external buffer with a low output impedance. $R_O$ may be lowered by adding a resistor from the output pin to $V_{EE}$. However, every 1mA of current drawn from the output pin may increase the buffer input current as much as 5-6 nA with consequent degradation in performance.

## Envelope Equations

**Attack Curve**

$$V_{OA} = V_Z \cdot (1-\exp(-\frac{t}{R_XC_X}e^{V_{CA}/V_T}))$$

**Decay Curve**

$$V_{OD} = (V_P-V_{CS})\exp(-\frac{t}{R_XC_X}e^{V_{CD}/V_T})+V_{CS}$$

**Release Curve**

$$V_{OR} = V_{CS}\exp(-\frac{t}{R_XC_X}e^{V_{CR}/V_T})$$

**Sustain/Release Final Voltage Error**

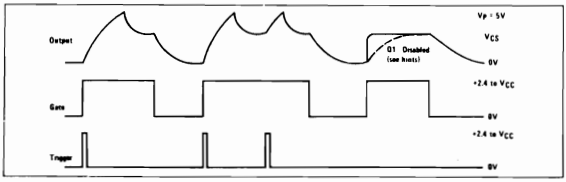
$$\epsilon_F = V_{OS} + I_{B1}R_X - I_{B2}R_X/1+e^{V_{CA}/V_T}$$

**Attack/Decay/Release Asymptote Error**

$$\epsilon_A = V_{OS} + I_{B1}R_X - I_{B2}R_X e^{-V_{CA,D,R}/V_T}$$

$V_{CA}$ = Attack Control Voltage
$V_{CD}$ = Decay Control Voltage
$V_{CR}$ = Release Control Voltage
$V_{CS}$ = Sustain Control Voltage
$V_{OS}$ = Op Amp Offset
$I_{B1}$ = Op Amp Input Current
$I_{B2}$ = Buffer Input Current
$V_Z$ = Attack Asymptote Voltage
$V_P$ = Envelope Peak Voltage
$V_T$ = kT/q

## Input and Output Waveforms



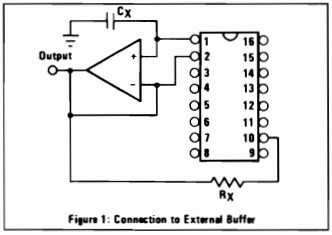




Figure 1: Connection to External Buffer

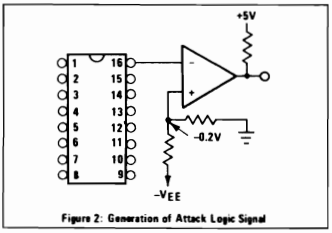



Figure 2: Generation of Attack Logic Signal

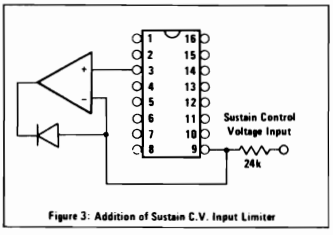



Figure 3: Addition of Sustain C.V. Input Limiter

### Use of External Buffer

For various reasons, it may be desired to use an external buffer. One possible benefit might be a lower input bias current ($I_{B2}$), with consequent improvement in the associated errors. The external buffer should be connected as shown in Figure 1. For proper operation, the buffer used should be capable of sourcing at least 700 μA and should have a positive current flowing into the input pin, such as that resulting from NPN or P channel JFET inputs.

### Disabling the Control Voltage Rejection Circuit

The purpose of Q1 (see block diagram) is to greatly reduce the control voltage feedthrough. During the attack phase, the base of Q1 is brought negative effectively disabling it and allowing Q2 to control the charging current. During the decay and release phases, however, the base of Q1 is at ground, causing negative voltage excursions on the base of Q2 to vary the charging current only a maximum of 2:1 (as opposed to the normal 10,000:1 or greater). Under normal triggering conditions (applying a trigger and a gate), this has no consequence, except to reduce the attack control voltage feedthrough to a negligible amount. However, if only a gate is applied with no trigger, the output will ramp up to the sustain level, approaching it asymptotically with a RC time constant of $R_X C_X(\exp(V_{CA}/V_T) + 1)$ (i.e. a rapid attack with only a 2:1 control range). To provide the normal full range of attack control under this mode of operation, Q1 should be disabled by connecting a resistor from pin 16 to $V_{EE}$ to generate at least -500mV at the base of Q2. This resistance may be calculated as follows:

$$R = 1100(2V_{EE}-1)$$

The result will be 5,000 times or more sustain and release final voltage shift with the attack control voltage. If external circuitry is added to apply the -500 mV only when the gate is high, then only the sustain final voltage will exhibit significant shift.

### Use of the Attack and Threshold Voltage Output Pins

The attack output pin (pin 16) and the peak threshold voltage pin (pin 3) have been provided to allow additional flexibility. Since pin 16 outputs a -.4 to -1.2 volts only during the attack phase, it may be used to provide a logic signal which indicates the attack phase (see figure 2). This signal may be ANDed with the gate to provide a logic signal indicating the decay phase. As was mentioned above, a sustain control voltage greater than the threshold voltage will result in a "jump" to the sustain level. By using the threshold voltage pin as shown in figure 3, the sustain voltage can be prevented from rising above the envelope peak, thus eliminating this undesirable effect. (This effect can also be eliminated by disabling the control voltage rejection circuit as described above).

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Covered by U.S. Patent #4,004,141. Printed in U.S.A. © 1979

Solid State Micro Technology for Music

ADVANCE INFORMATION

**SSM 2033**

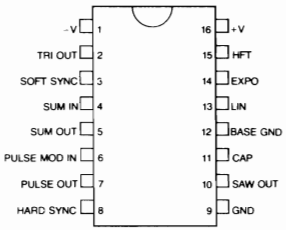
# VOLTAGE CONTROLLED OSCILLATOR*

## DESCRIPTION

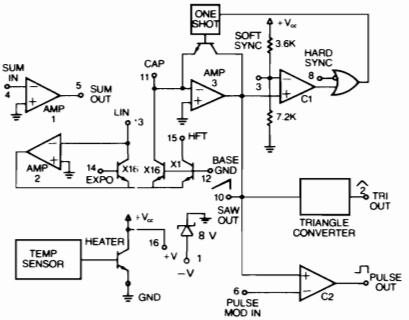
The SSM 2033 is a precision voltage controlled oscillator designed specifically for tone generation in electronic music. It has sawtooth, triangle, and variable width pulse outputs. Simultaneous exponential and proportional linear sweep inputs can control operating frequency over a 500,000-to-1 range. On-chip low input bias summer and control op amps have been provided. The pulse comparitor, which has built-in hysteresis for clean switching, can control pulse width duty cycle from 0 to 100%. Hard and soft sync inputs make possible a rich variety of modulation and harmonic locking effects. In addition, the operating temperature of the chip is regulated making external temperature compensation unnecessary. Only one trim (volts/octave) is required for normal operation.

## FEATURES

- Full on-chip temperature compensation.
- 500,000-to-1 sweep range.
- Simultaneous sawtooth, triangle, and variable width pulse outputs.
- Simultaneous exponential and proportional linear sweep inputs.
- On-chip summer and control op amps.
- Excellent exponential conformity.
- All outputs are short circuit protected.
- Hard and soft sync inputs.
- Pulse duty cycle voltage controllable from 0 to 100%
- Pulse comparitor has built-in hysteresis.
- 100 nsec sawtooth discharge time.
- Only volts/octave trim required for normal operation.




PIN OUT (TOP VIEW)




BLOCK DIAGRAM

**Solid State Micro Technology for Music, Inc.**, 20768 Walsh Avenue, Santa Clara, CA 95050, USA
**(408) 727-0917** Telex **171189**

*PATENTS APPLIED FOR

**SPECIFICATIONS***

25°C
$V_{CC}$ = +15, -V = Internal Reference

**OPERATING TEMPERATURE**

−10°C to +55°C

**STORAGE TEMPERATURE**

−55°C to +125°C

| PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Positive Supply Current | 8.0 | 10.5 | 13.3 | mA | |
| Max Heater Current(1) | 30.0 | 37 | 45 | mA | |
| Positive Supply Voltage Range | 9.0 | 15 | 18 | V | |
| Negative Supply Voltage Range(2) | −4.5 | −15 | −18 | V | |
| Sweep Range | 250K:1 | 1M:1 | | | |
| Integrator Input Bias Current | – | 0.3 | 1 | nA | |
| Control Circuit Offset | −5.0 | 0 | +5 | mV | |
| Max Operating Frequency | 270 | 330 | 440 | kHz | C = 1000 pf |
| Max Charging Current | 270 | 330 | 440 | μA | |
| Exponential Scale Error | – | 0.05 | 0.2 | % | $-90\ mV \leq V_e \leq +90\ mV$ |
| Sawtooth Peak Level | 9.75 | 10.0 | 10.25 | V | |
| Sawtooth Discharge Level | – | 200 | 350 | mV | |
| Sawtooth Discharge Time | – | 100 | – | n sec | |
| Sawtooth Output Short Circuit Current | 5.6 | 7.5 | 9.4 | mA | |
| Triangle Peak Level | 4.75 | 5.0 | 5.25 | V | |
| Triangle Trough Level | −250 | 0 | +250 | mV | |
| Triangle Output Short Circuit Current | 8 | 11 | 14 | mA | $V_{pin\ 2}$ = GND |
| Pulse Upper Level | 5.8 | 6.5 | 7.2 | V | |
| Pulse Lower Level | −100 | 0 | +100 | mV | Pin 7 has 15K to GND |
| Pulse Fall Time | – | 350 | – | n sec | |
| Pulse Rise Time | – | 200 | – | nsec | |
| Pulse Modulation Input Bias Current | 0.75 | 2.0 | 6.0 | μA | $V_{pin\ 6} > V_{pin\ 10}$ |
| Control and Summer Op Amps | | | | | |
| Input Offset Voltage | −5 | – | +5 | mV | |
| Input Offset Voltage Drift | – | 0.2 | – | μV/C° | 0°C ≤ T ≤ 45°C |
| Input Bias Current | – | 40 | 250 | μA | |
| Input Bias Current Drift | – | 50 | – | pA/C° | |
| Frequency Drift With Temperature | | | | | 0°C < T < 45°C |
| Basic Loop | −20 | – | +20 | ppm/C° | $V_e$ = GND |
| Over 1000-to-1 Sweep | −100 | – | +100 | ppm/C° | $V_e$ = ±90 mV |

**Notes:**

*Final specifications may be subject to change.

(1) Both circuit positive supply current and heater current appear at pin 16.

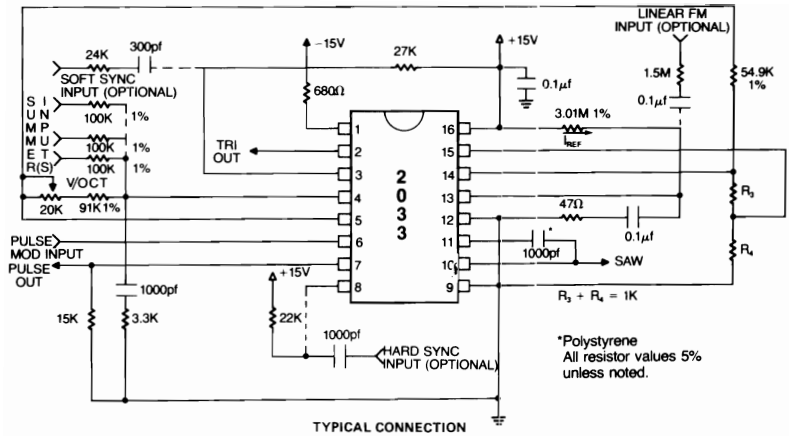
(2) Series current limiting resistor required for negative supplies greater than −6 V.

---

The schematic above show the typical connection of the SSM 2033 as an electronic music VCO. The control circuit section is redrawn for easy reference (figure 1). Any number of input voltages can be summed by amplifier $A_1$ which drives the exponential input attenuator to pin 14. Amplifier $A_2$ forces the current in $Q_1$ to be equal to the sum of the reference current, established by $R_1$, and the linear FM voltage. The current in the output transistor $Q_2$ is:

$$I_o = (V_+/R_1 + V_L/R_2)\, e^{-V_e q/kT} \qquad \frac{kT}{q} = 28.3\ mV\ @\ 55°C$$

Propagation delay and discharge time can cause a deviation from true exponentiality at high frequencies. To correct for this effect, transistor $Q_3$ provides feedback to the exponential control input. At low frequencies (currents), $Q_3$ will have a negligible effect on the voltage at the base of $Q_1$. At high frequencies (currents), $Q_3$ will correct for the tendency of the oscillator to track flat.




TYPICAL CONNECTION

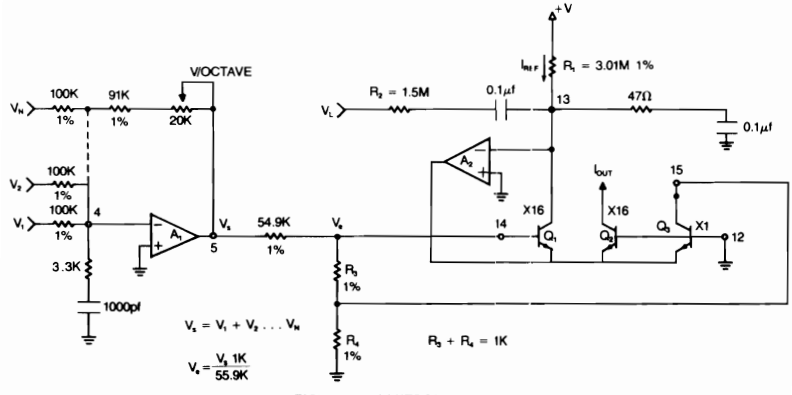



FIGURE 1 – CONTROL CIRCUIT

The SSM 2033 has an on-chip temperature sensor and heater which regulates the chip temperature to 55°C. The kT/q term in the exponent of the equation above is now a fixed value independent of ambient temperature. Operating temperature is reached 30 to 40 seconds after device power-up. Current drawn by the heater will decrease as ambient temperature rises. The temperature stabilization also insures that errors caused by offset drift with temperature in the summer and control op amps will be extremely small.

The output current of the control circuit is fed to an integrating amplifier which creates the sawtooth waveform. The instantaneous sawtooth output is compared to a reference voltage that is two-thirds of the positive supply. Sawtooth discharge is accomplished by a capacitorless one-shot which delivers a pulse to the discharge transistor when triggered by comparator $C_1$.

The triangle converter and pulse width comparator shape the sawtooth to provide the other two waveform outputs. The 27K resistor between the positive supply and the soft sync pin centers the sawtooth for proper triangle conversion. Comparator $C_2$ compares the pulse width modulation input voltage to the instantaneous sawtooth output to create a pulse that can have a duty cycle between 0 and 100%. The control range on the PWM input is between 0 and 10 V. $C_2$ has about 180 mV of built-in hysteresis to give fast clean transistions on both the rising and falling edges of the output.

The hard and soft sync features provide additional means for timbre modulation and additive synthesis. The hard sync input senses a falling edge, such as another 2033's sawtooth discharge, and forces an immediate discharge of the synced 2033. The resulting waveform has a complex harmonic structure whose pitch is that of the incoming oscillator (figure 2). The soft sync input also accepts a falling edge but it will force discharge only if the synced 2033 is within $240K/(R_3 + 2.4K)$ % of discharge. This enables one to phase-lock two oscillators to frequencies that are exact small integer ratios of one another (figure 3). By mixing the waveforms of the two oscillators, complex additive synthesis can be performed.

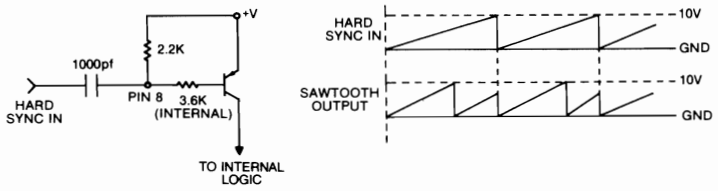



FIGURE 2 – HARD SYNC

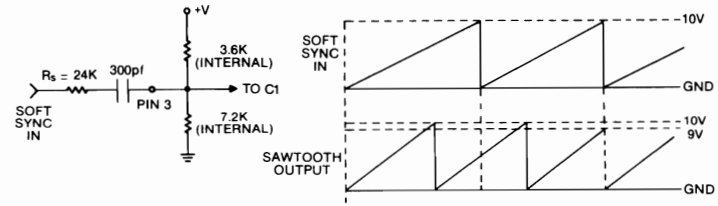



FIGURE 3 – SOFT SYNC

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Solid State Micro Technology for Music

ADVANCE INFORMATION

**SSM 2056**

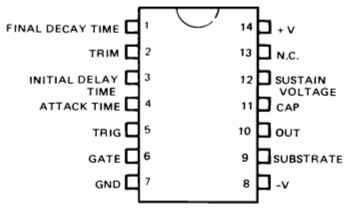
# VOLTAGE CONTROLLED TRANSIENT GENERATOR

## DESCRIPTION

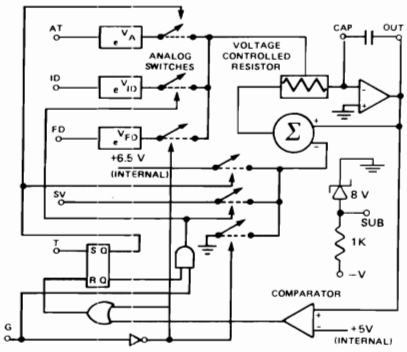
The SSM 2056 is a precision, self-contained, four section voltage controlled transient generator designed for easy use in programmable electronic music systems. The device offers near zero offset and control feedthrough, standard 5V peak output and an exponentially controlled 50,000 to 1 range on all timing inputs. Sustain voltage level can be varied from 0 to 100%. In addition, all control inputs are gangable and referenced from GND up allowing easy interface with electronic controllers and programmers.

## FEATURES

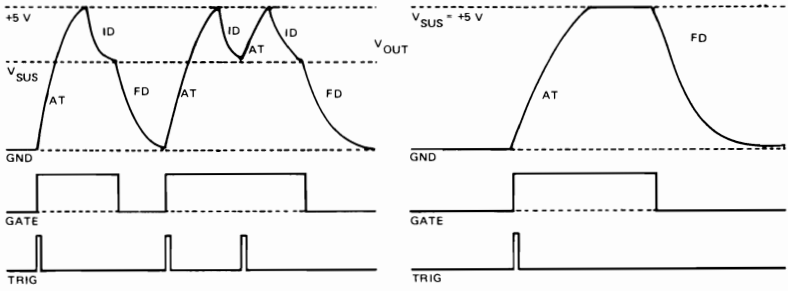
- Full ADSR Response
- Low Cost
- Independent Gate and Trigger
- Minimum external component count
- True RC contour
- ±15 V supplies
- Small fixed final decay and sustain voltage offset
- Output short circuit protected
- Negligible control feedthrough
- 5 V peak output
- Gangable control inputs
- Minimum 50,000 to 1 exponential time control range
- All input controls positive going from GND
- Output can drive heavy RC loads without degrading performance




PIN DIAGRAM – TOP VIEW




**Solid State Micro Technology for Music**, 2076B Walsh Avenue, Santa Clara, CA 95050, USA
**(408) 248-0917** Telex **17189**




## DIAGRAM DESCRIPTION

AT, ID, FD indicate times controlled by Attack, Initial Decay and Final Decay Time Control inputs respectively. (A positive going voltage increases the time constant.) All phases of the waveform are true exponential approaches to +6.5 V, Sustain Voltage and Ground respectively.

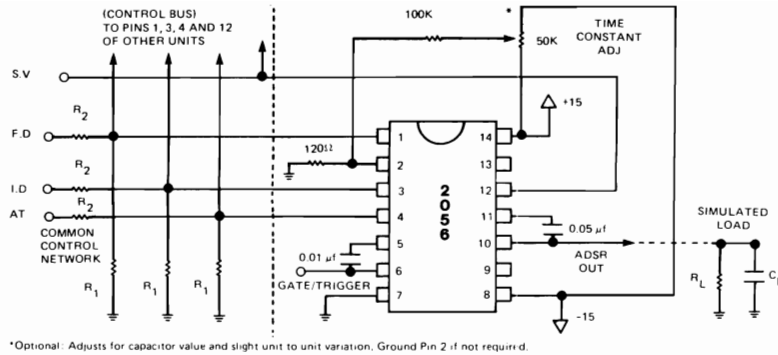
## ELECTRICAL SPECIFICATIONS* @ $V_S$ = ±15 and $T_A$ = 25°C

| PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|
| Positive Supply Current | 4.00 | 5.8 | 9.00 | mA | |
| Negative Supply Current | 6.0 | 8.65 | 12.0 | mA | Pin 8, $V_{ee}$ = −15 V |
| Positive Supply Range | +5 | +15 | +18 | V | |
| Negative Supply Range[1] | -4 | – | -18 | V | |
| Gate Threshold Voltage | 1.0 | 1.15 | 1.3 | V | |
| Gate Current (High) | -1 | 0 | +1 | μA | $V_G > 1$ V |
| Gate Current (Low) | – | -14 | -40 | μA | $V_G$ = GND |
| Trigger Threshold Voltage | 1.0 | 1.65 | 2.0 | V | |
| Trigger Input Inpendance | 5.14 | 6.85 | 8.56 | KΩ | $V_T > 0.8$ V |
| Trigger Threshold Current | 50 | 130 | 175 | μA | |
| Time Control Range | 50,000:1 | 250,000:1 | – | | |
| Time Control Sensitivity | – | + 60 | – | mV/Decade | |
| T.C. of Time Control Sensitivity | | + 3300 | | ppm/C° | |
| Unit to Unit Time Constant Variation (untrimmed) | 0.75 | 1 | 1.30 | | |
| Attack Voltage Asymtote | 6.3 | 6.5 | 6.7 | V | |
| Peak Attack Voltage | 4.9 | 5.0 | 5.1 | V | |
| Attack C. V Feedthrough | – | 0.5 | 2.5 | mV | $0 < V_{AT} < 240$mV |
| I.D. C. V Feedthrough | – | 0.5 | 2.5 | mV | $0 < V_{ID} < 240$mV |
| F.D. C. V Feedthrough | – | 3 | 13 | mV | $0 < V_{FD} < 240$ mV |
| Sustain Voltage Offset $V_o$-$V_{SV}$ | -13 | -18 | -23 | mV | At Final Value |
| Final Decay Offset $V_o$ | -13 | -18 | -23 | mV | At Final Value |
| Integrator Input Current | – | 0.1 | 1 | n A | |
| Sustain Voltage Input Current | – | 0.5 | 1.4 | μA | |
| Available Output Sink Current | 1.2 | 1.6 | 2.0 | mA | |
| Positive Output Short Circuit Current | 4.0 | 6.5 | 10.0 | mA | |

**NOTES**

*Final specifications may be subject to change.

(1)Pin 9 is used for negative supply voltages −4 V ≥ $V_{ee}$ ≥ −7 V.
Pin 8 is used for negative supply voltages −8 V ≥ $V_{ee}$ ≥ −18 V.




*Optional: Adjusts for capacitor value and slight unit to unit variation. Ground Pin 2 if not required.

TYPICAL CONNECTION

---

The diagram above shows the typical connection for a polyphonic system. The control attenuators on the left are common to all 2056's used for the same function within a voice; such as control of the final VCA. The sense of the control is from Ground up with minimum time periods at GND and increasing times at positive voltages. Some recommended resistor values for often-used sensitivities are given along with the general design equations below. The temperature coefficient of the time sensitivities can be compensated by using Tel Labs type Q81C resistors for the $R_1$'s.

The time constant adjustment is necessary in polyphonic systems to make all voices sound the same for long attack times. The procedure is to set the AT control for the longest required attack time, ground I.D., F.D. and S.V., and adjust each 2056 to give exactly the same attack period; 10 to 20 seconds is about the longest that is musically useful. The adjustment can be ignored in manually controlled monophonic systems.

The Gate/Trigger input(s) can be driven directly from the outputs of all TTL and CMOS logic families. The ADSR output can drive any grounded load $R_L > 2.5K$, $C_L < 5000pf$.

---

**Design Equations**

$$t_A = 0.5m \sec\dagger\left\{e^{+\frac{V_a R_1 q}{(R_1 + R_2)\, kT}} + 1\right\}$$

$$t_{ID} = 0.5m \sec\dagger\left\{e^{+\frac{V_{ID} R_1 q}{(R_1 + R_2)\, kT}} + 1\right\}$$

$$t_{F.D.} = 0.5m \sec\dagger\left\{e^{+\frac{V_{FD} R_1 q}{(R_1 + R_2)\, kT}} + 1\right\}$$

$$\frac{kT}{q} = 26mV \text{ @ } 25°C$$

**Design Table**

| Input Sensitivity | $R_1$ | $R_2$ |
|---|---|---|
| 1V/Decade | 60Ω†† | 940 Ω |
| 1V/Octave | 60Ω†† | 3.3kΩ |
| 1V/Decade | 100Ω | 1.5kΩ |
| 1V/Octave | 100Ω | 5.4kΩ |
| 1V/Decade | 250Ω | 3.9kΩ |
| 1V/Octave | 250Ω | 13.6kΩ |

**NOTES**

†Nominal Time Period with $V_{AT} = V_{ID} = V_{FD} = 0V$ and $C_T = 0.05\mu f$ is 1m sec.

††Tel Labs Type Q81C = 60 Ω @ 25°C  $R_1$ should be kept as small as possible when the control attenuator is driving many units.

# CEM 3330/3335

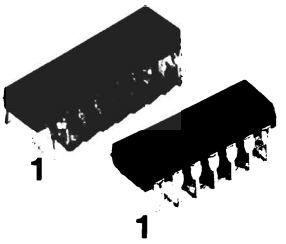
CURTIS ELECTROMUSIC SPECIALTIES
2900 Mauricia Ave.
Santa Clara, CA 95051
(408)247-8046

## Dual Voltage Controlled Amplifier

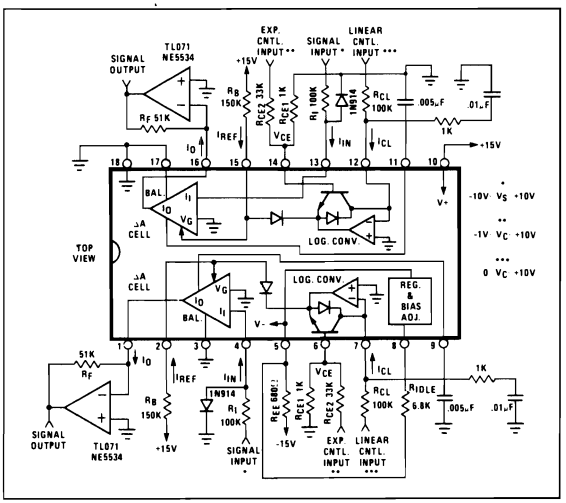
The CEM 3330 and CEM 3335 are dual, high performance, voltage controlled amplifiers intended for electronic musical instrument and professional audio applications. For the 3330, each amplifier includes complete circuitry for simultaneous linear and exponential control of gain. In addition, the operating point of the amplifiers may be set anywhere from Class B to Class A, allowing the user to optimize those parameters critical to the particular application. Also featured are virtual ground summing nodes for both the signal and linear control inputs, so that signal and control mixing may be accomplished within the device itself. Finally, the VCA outputs are signal currents, allowing the device to be conveniently used in two-pole voltage controlled filters, as well as dual voltage controlled amplifiers.

The 3335 is the same device as the 3330 but without the linear control circuitry, and is intended for those applications which require only the exponential control of gain.

The devices include an on-chip 6.5 volt Zener, allowing them to operate off ±15 volt supplies as well as +15, -5 volt supplies.




### CEM 3330 Circuit Block and Connection Diagram




### Features

- Low Cost
- Two Independent Voltage Controlled Amplifiers in a Single Package
- Simultaneous Linear and Exponential Control Inputs
- Wide Control Range: 120dB min.
- Very Accurate Control Scales for Excellent Gain Tracking
- Exceptionally Low Control Voltage Feedthrough: -60dB minimum without trim, better than -80dB with trim
- Low Distortion: Less than 0.1%
- Exceptionally Low Noise: Better than -100dB
- Class B to Class A Operation
- Summing Signal and Linear Control Inputs
- Current Outputs for Ease of Use in Voltage Controlled 2-Pole Filters
- Can Be Used in VCO and VCF Control Paths Without Causing Shift
- ±15 Volt Supplies

# CEM 3330 / CEM 3335

## Electrical Characteristics

| $V_{CC}$ = +15V | | $T_A$ = 25°C | | | |
|---|---|---|---|---|---|
| Parameter | Conditions | Min | Typ | Max | Units |
| Exponential Control Range | | 120 | 150 | – | dB |
| Linear Control Range | | 100 | 130 | | dB |
| Peak Cell Current, $I_{CP}$ | Class B | ±400 | ±600 | – | µA |
| (input plus output) | Class A | ±800 | ±1400 | – | µA |
| Exponential Control Scale Sensitivity | | 2.8 | 3.0 | 3.2 | mV/dB |
| Tempco of Exponential Control Scale | | +3000 | +3300 | +3600 | ppm |
| Tempco of Linear Control Scale | | – | ±100 | ±300 | ppm |
| Exponential Control Scale Error[1] | | – | 0.3 | 1 | dB |
| Linear Control Scale Error[1] | 0< $I_{CL}$ <100µA | – | 0.3 | 1.5 | % |
| Cell Current Gain | $V_G$ = 0 | .83 | 1 | 1.2 | |
| Current Gain Tempco | $V_G$ = 0 | – | ±100 | ±300 | ppm |
| Log Converter Output | $I_{CL} = I_{REF}$ | -5 | 0 | +5 | mV |
| Output Voltage Compliance | | -3 | – | +13.5 | V |
| Untrimmed Distortion[2] | Class B | – | 1.5 | 5 | % |
| | Class A | – | 0.3 | 1 | % |
| Trimmed Distortion[2] | Class B | – | 0.2 | 0.8 | % |
| | Class A | – | 05 | 0.2 | % |
| Untrimmed Control Feedthrough[3] | Class B | – | 0.2 | 0.8 | µA |
| | Class A | – | 7 | 25 | µA |
| Trimmed Control Feedthrough[3] | Class B | – | .01 | .08 | µA |
| | Class A | – | 1 | 5 | µA |
| Output Noise Current in 20KHz | Class B | – | 1.2 | 3.5 | nARMS |
| Bandwidth ($V_G$ = 0) | Class A | – | 3.5 | 12 | nARMS |
| Signal Current Bandwidth[4] | Class B | 30 | 100 | – | KHz |
| | Class A | 100 | 350 | – | KHz |
| Signal Current Slew Rate | Class B | 60 | 150 | – | µA/µS |
| | Class A | 400 | 750 | – | µA/µS |
| Crosstalk Between VCAs | F = 10KHz | -60 | -70 | – | dB |
| Internal Bias Current at Signal & Linear | Class B | 80 | 175 | 350 | nA |
| Control Inputs | Class A | 130 | 300 | 600 | nA |
| Exponential Control Input Current | $I_{CL}$ = 100µA | 4 | 0.8 | 1.3 | µA |
| Linear Control Input Offset Voltage | | -7 | +3 | +15 | mV |
| Signal Input Offset Voltage | | -15 | -5 | +5 | mV |
| Positive Supply Current | Class B | 0.8 | 1.3 | 2.1 | mA |
| | Class A | 2.1 | 2.7 | 3.7 | mA |
| Positive Supply Range | | +9 | – | +18 | V |
| Negative Supply Range[5] | | -4.5 | – | -18 | V |

**Note 1**: From current gains of +20dB to -80dB. Peak cell current is less than 100µA.
**Note 2**: Output signal is 10dB below clipping and is at a frequency of 1KHz. $V_G$ = 0
**Note 3**: Current gain varies from unity to maximum attenuation (>110dB).
**Note 4**: Peak Output Current is ±200µA.
**Note 5**: Current limiting resistor required for negative voltages greater than -6 volts.
**Note 6**: Class B is defined at an idle current of 1µA; Class A is at an idle current of 100µA

## Application Hints

### Supplies

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ±10% Zener diode has been provided to allow the chip to run off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 5). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 5 and the supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2)/I_{EE}$$

where $I_{EE}$ is .010 for idle currents less than 10µA, .012 for idle currents between 10µA and 50µA, and .014 for idle currents between 50µA and 200µA. (See Selection of Quiescent Operating Current).

Although the circuit was designed for a positive supply voltage of +15 volts, it may be operated from any voltage between +9 and +18 volts with little effect on performance.

### Basic Operation

Each of the two voltage controlled amplifiers consists of a variable gain cell and, in the case of the 3330, a log converter as well (see Block Diagrams). The gain cell is the current-in, current-out type, accepting a bipolar input current, $I_{IN}$, and providing a bipolar output current, $I_O$, with the following relationship:

$$I_O = -I_{IN} e^{-V_G/V_T} \qquad V_T = KT/q$$

where $V_G$ is the voltage applied to the direct control input of each gain cell (pin 2 and pin 15 on the 3330, pin 2 and pin 11 on the 3335).

For the 3330, the log converter generates the logarithm of the linear control input current,

$I_{CL}$, (pin 7 and pin 12) while transmitting the exponential control input, $V_{CE}$, (pins 6 and 14) unchanged to its output. The transfer function for each log converter is:

$$V_{OLC} = -V_T \ln \frac{I_{CL}}{I_{REF}} + V_{CE} = V_G$$

where $I_{REF}$ is the current sourced into the direct control input. Since the output of the log converter internally connects to the direct control input of the gain cell, the overall current gain of the gain cell is given by:

$$I_O = -I_{IN} \cdot \frac{I_{CL}}{I_{REF}} \cdot e^{-V_{CE}/V_T}$$

For proper operation, the linear control current, $I_{CL}$, and reference current, $I_{REF}$, are positive in polarity; that is, they flow into the device. A negative input current for $I_{CL}$ will simply shut the gain completely off, while a negative reference current should be avoided. The signal input current may, of course, be either polarity.

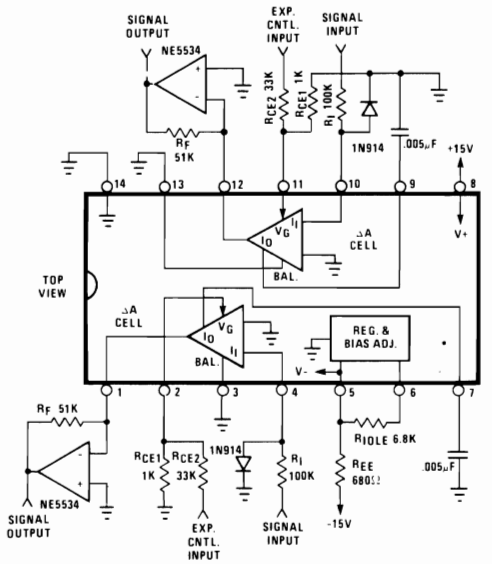
The Block Diagrams show typical external components connections to the devices. The signal inputs and the linear control inputs are virtual ground summing nodes; therefore, the signal input currents and linear control currents may be accurately generated from their respective voltages simply with resistors terminating at these nodes. Note that these virtual ground inputs also allow multiple input voltages to be mixed (linearly added) on-chip by merely adding more input resistors.

Although the voltage compliance of the gain cell outputs ranges from -0.3V to $V_{CC}$ - 1.5V, best results are obtained by feeding the outputs into virtual ground inputs. Thus, in the Block Diagrams, the output currents are converted to voltages with external op amps.

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage Between $V_{CC}$ and $V_{EE}$ Pins | +24V,-0.5V |
| Voltage Between $V_{CC}$ and Ground Pins | +18V,-0.5V |
| Voltage Between $V_{EE}$ and Ground Pins | -6.0V,+0.5V |
| Voltage Between Output and Distortion Trim or Ground Pins | +18V,-0.5V |
| Voltage Between All Other Pins and Ground Pin | ±6.0V |
| Current Through Any Pin | ±40mA |
| Storage Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -25°C to +75°C |

## CEM3335 Circuit Block and Connection Diagram



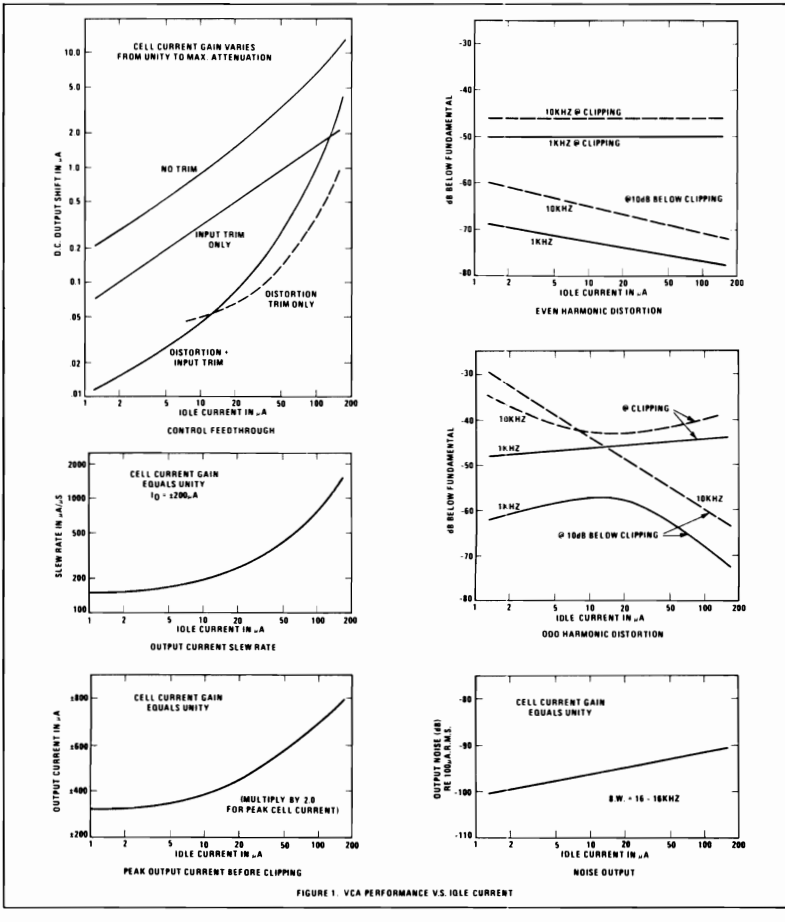



FIGURE 1. VCA PERFORMANCE VS. IDLE CURRENT

## Selection of Component Values

Selection of the input and output resistor values requires consideration of the preferred and maximum operating current levels of the device as well as the available input voltages and desired output voltage. In general, the input signal current should be made as large as possible to obtain the best signal to noise ratio. However, for either peak inputs currents or peak output currents greater than several hundred microamperes, distortion begins to increase significantly, until the total cell current (input peak current plus output peak current) exceeds the maximum value specified in the specifications for $I_{CP}$. At this point, clipping occurs, resulting in severe distortion.

For optimum noise performance, it is recommended that the input resistor, $R_I$, be selected so that the maximum *peak* input signal voltage causes ½ the peak cell current to flow in the input:

$$R_I = V_{IN\ MAX}/½\ I_{CP}$$

Note that the input could handle up to 6dB more current, but the cell current gain would have to be reduced so significantly to prevent clipping, that the signal to noise ratio would actually be degraded. (Output noise increases roughly by the square root of an increase in cell current gain). If more than one signal is being summed in the input, then the total of all peak input currents should be no greater than ½ $I_{CP}$. Next, the output resistor, $R_F$, is selected so that the desired maximum for the peak output voltage before clipping is produced with the maximum input signal. Thus,

$$R_F = V_{O\ MAX}/½\ I_{CP}$$

Note that the cell current gain for these conditions is unity, but the voltage gain for the circuit is $R_F/R_I$ and may be greater or less than unity. Note also that the current gain may be made greater than unity for inputs less than $V_{IN\ MAX}$.

Although $R_I$ and $R_F$ have been selected using maximum input and output conditions, the device should nominally operate at least 6 to 20 dB below these maximum levels (corresponding to 100μA or less input and output currents) for best distortion performance.

With the values of $R_I$ and $R_F$ selected, the maximum linear control current, $I_{CL}$, and most negative exponential control voltage, $V_{CE}$ ($V_G$ in the case of the 3335), are selected to give the maximum desired voltage gain in accordance to the following equations:

$$A_{V\ 3330} = \frac{R_F}{R_I} \cdot \frac{I_{CL}}{I_{REF}} \cdot e^{-V_{CE}/V_T}$$

or

$$A_{V\ 3335} = \frac{R_F}{R_I} \cdot e^{-V_G/V_T}$$

The maximum gain is only limited by either the total cell current exceeding $I_{CP}$, or excessive noise and DC output shift with cell current gains much greater than unity (>+40dB).

For greatest linear scale accuracy, the maximum value of $I_{CL}$ should be restricted to 100μA or less, although currents up to 300μA can be used with increasing error. For best distortion performance, the reference current, $I_{REF}$, should also be set between 50μA and 200μA; it may be generated simply with a resistor to $V_{CC}$. The linear control input resistor, $R_{CL}$, is thus selected so that the maximum available linear control voltage produces the desired maximum value for $I_{CL}$.

Finally, the selected value of $I_{REF}$ together with $I_{CL\ MAX}$ determines the most negative value of $V_{CE}$ required to generate the maximum voltage gain. If the exponential input is not used, then it may be grounded ($V_{CE}$ = 0), and only the values of $I_{CL\ MAX}$ and $I_{REF}$ juggled to obtain the maximum gain factor.

## Selection of the Quiescent Operating Current

A unique feature of the device is that the quiescent standby, or idle, current of the signal-carrying transistors can be set anywhere between one and several hundred microamperes, thus effectively allowing the user to set the operation of the gain cells anywhere between Class B and Class A. Since the quiescent operating point affects all VCA characteristics, improving some while worsening others, the idle current is selected to optimize those parameters important to the particular application.

As shown in the graphs of Figure 1, increasing the idle current decreases distortion, improves slew rate, and increases available output current, but all at the expense of increased noise and greater control voltage feedthrough. Thus, if the application is to control the level of low frequency control signals where control voltage rejection is critical, then the VCA is best operated Class B. For the processing of audio signals, however, the VCA should be operated Class AB to Class A, with the best compromise between distortion, noise and bandwidth.

The quiescent idle current is set the same for both VCAs by placing a resistor between the idle adjust pin (pin 8 on the 3330, pin 6 on the 3335) and the $I_{EE}$ pin (pin 5). Figure 2 shows the idle current versus the value of this resistor. With

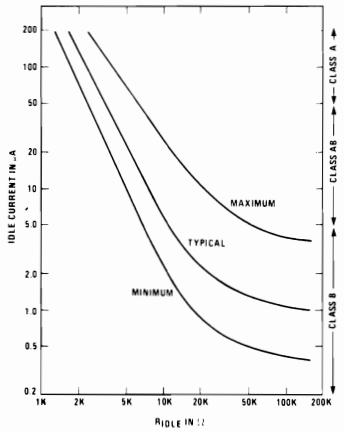



FIGURE 2 IDLE CURRENT VS IDLE ADJUST RESISTOR

no resistor ($R_{IDLE} = \infty$) the idle current is typically at 1$\mu$A and the VCAs will operate Class B.

As can be seen from Figure 2, the idle current may vary significantly from device to device for any given value of $R_{IDLE}$, due to the ±25% tolerance of the internal resistors. In most cases, this idle current tolerance is acceptable because the VCA parameters will vary to a much lesser extent. However, the idle current may be set more precisely by measuring the idle current and adjusting the value of $R_{IDLE}$ with a trim pot until the desired value is obtained. The idle current is measured by measuring the output current with no signal input and at a current gain of unity while putting roughly -0.5 to -1.5 volt on the distortion trim pin (pins 3 and 17 on the 3330, pins 3 and 13 on the 3335).

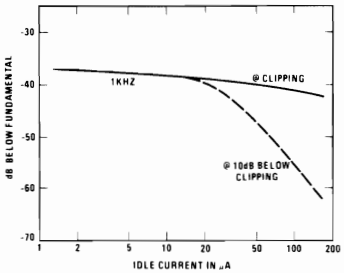



FIGURE 3: SECOND HARMONIC DISTORTION, UNTRIMMED

## Trimming of the Second Harmonic Distortion

When operating the VCAs less than Class A, internal transistor mismatches will cause the gain during the positive portion of the input signal to differ from that during the negative portion, thus introducing even harmonic distortion (predominantly second). In Figure 3 is shown a graph of typical untrimmed second harmonic distortion (distortion trim pins connected to ground) versus the idle current. This distortion may be acceptable in some applications, but will have to be trimmed out in others. Trimming is accomplished by adjusting the voltage on the distortion trim pins (pins 3 and 17 on the 3330, pins 3 and 13 on the 3335) somewhere between ±10mV, as shown in Figure 4.

The even harmonic distortion may be trimmed to near minimum with the following simple procedure: The signal input is alternately switched between ground, a positive voltage source (such as a battery) and a negative voltage source of the *exact* same magnitude (best accomplished by simply reversing the leads to the positive voltage source). The value of the voltage source is selected to be equal to the peak signal level at which it is desired to trim the distortion. The output voltage is measured to four digits with a DVM for each of the three input conditions, and the trim adjusted so that the output voltage change is the same going from the grounded to positive input as it is going from the grounded to negative input.

Although the second harmonic may be trimmed out to better than 80dB at almost any gain setting and input signal level, it is best to perform the trimming at a current gain of zero and input signal level around 10dB below the clipping point. This procedure will yield, in general, the best distortion performance at all input levels and gain settings except at the very highest (last 10 to 6dB before clipping at the output). And since in the case of the music and speech signals, the last 15 to 20dB should be reserved for headroom, this result is acceptable.

As most of the odd order harmonic distortion is due to crossover distortion, there is no way to trim it out; it may be reduced only by increasing the idle current.

## Optimizing the Bandwidth

As can be seen from the Block Diagrams, the log converters are stabilized with a series 1K resistor and .01$\mu$F capacitor compensation network from the linear control input to ground, while each of the gain cells may be compensated with a .005$\mu$F capacitor from the compensation pins (pins 9 and 11 on the 3330, pins 7 and 9 on the 3335) to ground. This gain cell compensation is good for low frequency control applications, but may result in inadequate large signal bandwidth for quality audio applications.

Figure 5 shows an improved compensation technique for

greater bandwidths and slew rate: By placing a series 1K resistor and .01$\mu$F capacitor network from the signal input to ground, the .005$\mu$F compensation capacitors may be reduced to 150 pF, resulting in the bandwidths and slew rate shown in Figure 1.

## Control Inputs

As was discussed earlier, the linear control input resistor, $R_{CL}$, should be selected so that the linear control current reaches a maximum of 50$\mu$A to 200$\mu$A. This level is low enough so as not to cause significant control scale non-linearity, but high enough to swamp out the effects of the internal input bias current. Since the actual current controlling the linear gain is the input control current minus this bias current, the input control voltage at which the gain becomes zero is given by:

$$V_{CLO} = I_B R_{CL} + V_{OS}$$

This cut-off point may be increased by injecting a small constant negative current into the control input, or decreased by injecting a small positive current into the input.

As the scale sensitivity of the exponential control inputs on both the 3330 and 3335 are 18mV/-6dB, an attenuation network will in most cases by required. An increasing positive control voltage decreases the gain.

The basic gain cell is fully temperature compensated. The only first order temperature effect is the exponential control factor tempco ($1/V_T$). This effect may be substantially reduced by using a +3300ppm tempco resistor (Tel Labs Q81) for $R_{CE1}$, shown in the Block Diagrams. If only the linear control input is to be used, then the exponential input is grounded and no temperature compensation is necessary.

To use the 3330 for exponential gain control only, the entire log converter may be bypassed, reducing the number of external components and potential errors introduced by the log converter. This is accomplished by simply leaving the linear and exponential control inputs open, and applying the exponential control voltage directly to the $I_{REF}$ pin (which is also the direct input, $V_G$, to the gain cell) as shown in Figure 6. The scale sensitivity is the same as that of the exponential input to the log converter, and therefore requires the same considerations as discussed above.

For best distortion performance, it is recommended that the impedance at both the distortion adjust inputs and direct control inputs (3330 or 3335) be kept below several hundred ohms.

## Trimming of the Control Voltage Feedthrough

The shift in the quiescent DC output voltage as the gain is changed is due to several factors. One cause is the internal bias current at the signal current input, being only of concern at idle currents less than 10$\mu$A. The other cause is the same potential imbalance between the two signal processing halves which also is responsible for even order harmonic distortion.

Thus, there are two methods for minimizing the control voltage feedthrough: One is to inject an adjustable DC current into the signal current input pin, as shown in Figure 7. The range of this current should be roughly equal to plus and minus the idle current. (For idle currents less than 5$\mu$A, it is not necessary that this current be adjustable to negative values.) The best technique for adjusting this trim for maximum control voltage rejection is to simply set the gain to maximum and adjust the pot for zero DC quiescent output current. (The DC output current at zero gain is always zero.)

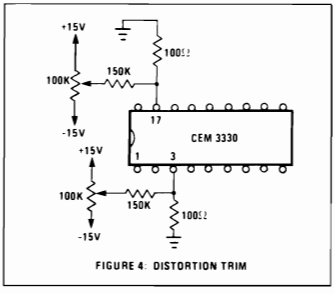


FIGURE 4: DISTORTION TRIM

The other method for minimizing control voltage feedthrough is to balance the two circuit halves by adjusting the second harmonic distortion trim discussed above. This method, although usually reducing the distortion below that of the untrimmed value, will not adjust

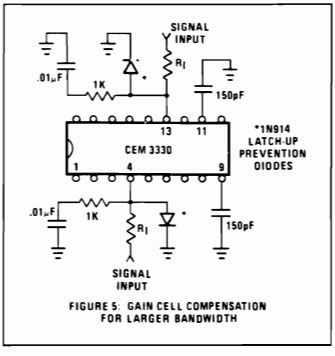


FIGURE 5: GAIN CELL COMPENSATION FOR LARGER BANDWIDTH

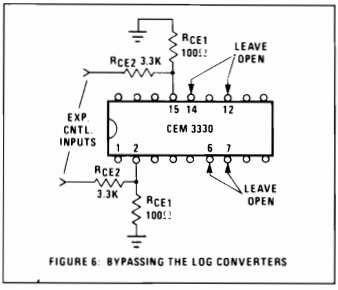



FIGURE 6: BYPASSING THE LOG CONVERTERS

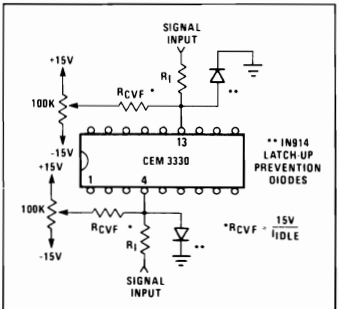



FIGURE 7: CONTROL REJECTION TRIM

the distortion to its potential minimum. Conversely, minimizing the distortion with this trim does not necessarily minimize the control voltage feedthrough. (At high values of idle current, it may even increase it.) The technique for using this trim to maximize the control rejection is the same as before: the pot is adjusted for zero DC current output at maximum gain.

At idle currents less than 10μA, it is recommended that the input trim of Figure 7 be used rather than the distortion trim, as the distortion trim tends to increase the distortion above the untrimmed value when feedthrough has been minimized. At higher idle currents, however, it is recommended that the distortion trim be used to minimize feedthrough, since it will also tend to reduce distortion below the untrimmed value. In fact, this is a good method for improving (but not necessarily optimizing) both distortion and control rejection with only a single trim. For absolute best control voltage rejection, where the distortion is not as critical as control rejection, it is recommended that both the input current adjust of Figure 7 and the distortion trim be simultaneously adjusted to produce minimum feedthrough.

Shown in Figure 1 are typical values of control feedthrough versus idle current for untrimmed, trimmed with the input current adjust only, trimmed with the distortion adjust only, and trimmed with the input adjust after the distortion has been trimmed for minimum.

For best overall VCA performance at any idle current, where both distortion and feedthrough are important, it is recommended that the second harmonic distortion is first trimmed for minimum, and then the control voltage feedthrough trimmed with the technique of Figure 7.

## Layout Considerations

In the usual case where the outputs connect to the summing inputs of op amps, these output traces should be kept short to prevent their high impedance from picking up extraneous signals.

Since capacitance greater than 50pF at the idle adjust pin may cause high frequency oscillation, care should be exercised in the layout to minimize stray capacitance at this pin.

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# CEM 3340 / 3345

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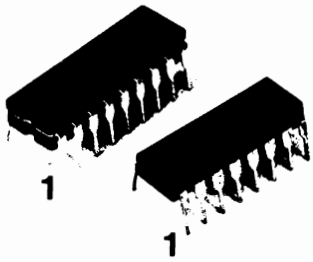
## Voltage Controlled Oscillator

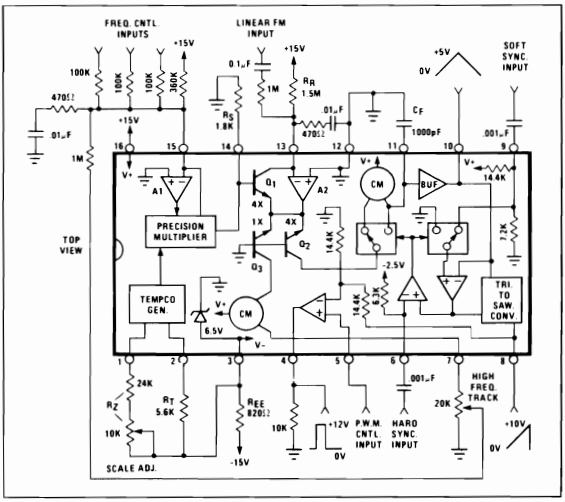
The CEM 3340 and CEM 3345 are completely self contained, precision voltage controlled oscillators, featuring both exponential and linear control scales and up to four buffered output waveforms: triangle, sawtooth, square, and pulse with voltage controllable pulse width. Full temperature compensation makes these VCOs extremely stable, and eliminates the need for a temperature compensation resistor. The highly accurate exponential and linear control inputs are virtual ground summing nodes, allowing multiple control voltages to be mixed within the device itself.

Also included is provision for hard and soft synchronization of the frequency, and an output for easy adjustment of high frequency tracking. Special care in the design ensures oscillation start-up under any power-on sequence and supply conditions.

Although a low voltage process has been used to reduce die size, cost, and leakage currents, an on-chip 6.5 volt zener diode allows the device to operate off ±15 volt supplies, as well as +15,-5 volt supplies.




### CEM 3340 Circuit Block and Connection Diagram




**Features**

- Large Sweep Range: 50,000:1 min.
- Fully Temperature Compensated; No Q81 Resistor Required
- Four Output Waveforms Available; No waveform trimming required.
- Summing Node Inputs for Frequency Control
- High Exponential Scale Accuracy
- Low Temperature Drift
- Voltage Controlled Pulse Width
- Hard and Soft Sync Inputs
- Linear FM
- Buffered, Short Circuit Protected Outputs
- ±15 Volt Supplies

# CEM 3340 / CEM 3345

## Electrical Characteristics

| $V_{CC}$ = +15V $V_{EE}$ = Internal Zener $T_A$ = 20°C | | | | |
|---|---|---|---|---|
| Parameter | Min. | Typ. | Max. | Units |
| Frequency Control Range | 50K:1 | 500K:1 | – | |
| Exponential Scale Error, Untrimmed[1] | – | 0.2 | 1 | % |
| Exponential Scale Error, Trimmed[1] | – | 0.05 | 0.3 | % |
| Multiplier Gain Error[2] | – | 0.0005 | 0.008 | %/μA |
| Tempo Cancellation[3] | -150 | 0 | +150 | ppm |
| Oscillator Drift[4] | – | ±50 | ±200 | ppm |
| Triangle Buffer Input Current | – | 0.3 | 3 | nA |
| Triangle Waveform Upper Level | 4.85 | 5.0 | 5.15 | V |
| Triangle Waveform Lower Level | -15 | 0 | +15 | mV |
| Triangle Waveform Symmetry | 45 | 50 | 55 | % |
| Sawtooth Waveform Upper Level | 9.4 | 10.0 | 10.6 | V |
| Sawtooth Waveform Lower Level | -25 | 0 | +25 | mV |
| Triangle Output Sink Capability | 400 | 550 | 750 | μA |
| Sawtooth Output Sink Capability | 640 | 800 | 1000 | μA |
| Triangle & Sawtooth Output Impedance[5] | 65 | 100 | 150 | Ω |
| Pulse Output Source Capability at +10V | 2.8 | 3.5 | 4.6 | mA |
| Squarewave Output Levels[6], CEM 3345 | -1.8,-0.4 | -1.3,0 | -0.8,+0.4 | V |
| PWM Input Pin Current[7] | .5 | 1.5 | 3.5 | μA |
| PWM Input Voltage for 0% Pulse Width | -15 | 0 | +15 | mV |
| PWM Input Voltage for 100% Pulse Width | 4.6 | 5.0 | 5.4 | V |
| Input Bias Current at Reference and Control Current Inputs | 80 | 200 | 400 | nA |
| Tempco of Input Bias Currents | -1000 | 0 | +1000 | ppm |
| Offset Voltage at Reference and Control Current Inputs | -5 | 0 | +5 | mV |
| Hard Sync Reference Voltage | -2.3 | -2.5 | -2.8 | V |
| Hard Sync Input Resistance | 5 | 6.3 | 7.9 | KΩ |
| Max Capacitor Charge/Discharge Current | 400 | 570 | 800 | μA |
| Positive Supply Current | 4 | 5 | 6.5 | mA |
| Positive Supply Voltage Range | +10 | | +18 | V |
| Negative Supply Voltage Range[8] | -4.5 | | -18 | V |

**Note 1:** This error represents the percentage difference in scale factors (volts per frequency ratio) of the exponential generator anywhere over the exponential generator current range of 50nA to 100μA. Most of this error occurs at the range extremities.

**Note 2:** This error represents the percentage difference in multiplier gains at any two input currents, within the range of 20 μA to 180 μA, per μA difference between the two corresponding outputs.

**Note 3:** This spec represents the difference between the actual tempco of the multiplier output voltage (expressed relative to the maximum output excursions) and the tempco required to precisely cancel the tempco of the exponential scale factor (q/KT).

**Note 4:** The multiplier output is grounded.

**Note 5:** For exponential generator currents less than 10 μA; above 10 μA, impedance drops to 1/3 this value as the highest current is approached.

**Note 6:** With respect to the hard sync input reference voltage.

**Note 7:** For PWM control inputs between -1 and +6 volts. This current is significantly greater for inputs outside of this range.

**Note 8:** Current limiting resistor required for negative supplies greater than -6 volts.

## Application Hints

### Supplies

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ± 10% Zener diode has been provided to allow the chip to operate off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 3). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 3 and the negative supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2) / .008$$

Although the circuit was designed for a positive supply of +15 volts, it may be operated anywhere between +10 and +18 volts. The only effect is on the positive peak amplitude of the output waveforms in accordance to the following: The triangle peak is one third of the supply, the sawtooth peak is two thirds of the supply, and the pulse peak is 1.5 volts below the supply.

### Operation of the Temperature Compensation Circuitry

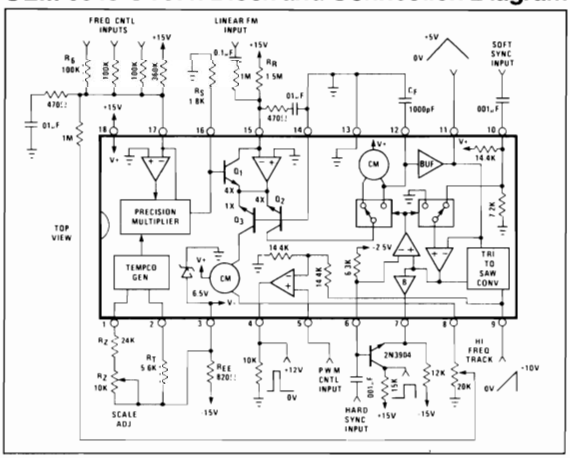
The exponential generator is temperature compensated by multiplying the current sourced into the frequency control pin (pin 15 on the CEM3340, pin 17 on the CEM3345) times a coefficient directly proportional to the absolute temperature. As this control current is applied to the exponential generator, its coefficient cancels that of the exponential generator, q/KT. This coefficient is produced by the tempco generator using the same mechanisms that create it in the exponential generator; cancellation is therefore nearly perfect.

The output of the precision multiplier (pin 14 on the 3340,

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage Between $V_{CC}$ and $V_{EE}$ Pins | +24V,-0.5V |
| Voltage Between $V_{CC}$ and Ground Pins | +18V, -0.5V |
| Voltage Between $V_{EE}$ and Ground Pins | -6.0V,+0.5V |
| Voltage Between Frequency Control Pin or Reference Current Pin and Ground Pin | ±6.0V |
| Voltage Between Multiplier Output Pin and Ground Pin | +6.0V, -1V |
| Current through Any Pin | ±40mA |
| Storage Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -25°C to +75°C |

## CEM 3345 Circuit Block and Connection Diagram




pin 16 on the 3345) internally connects to the control input of the exponential generator (base of $Q_1$). This output is a current and is given by:

$$I_{OM} = \frac{22V_T}{R_T}\ (1 - I_C R_Z/3.0)$$

where $V_T = KT/q = 26$ mV @ 20°C, and where $I_C$ is the total current flowing into the frequency control pin and must remain positive for proper operation (a negative input current will produce the same output as a zero input current). Since the frequency control input pin is a virtual ground summing node, any number of control voltages may be summed simply with input resistors to this pin.

The current output of the multiplier is converted to the required drive voltage with a resistor from the multiplier output pin to ground. For greatest multiplier accuracy, this resistor, $R_S$, should be 1.8k and the current flowing out of pin 2, $22V_T/R_T$, should be close to the current flowing out of pin 1, $3.0/R_Z$.

Since the components associated with the tempco generator and multiplier determine the maximum voltage excursion possible at the base of $Q_1$, they should be selected to provide the desired frequency control range of the oscillator. The exponential generator itself is capable of delivering a current for charging and discharging the timing capacitor from greater than .5mA down to less than the input bias current of the buffer, thus allowing for a typical frequency range greater than 500,000:1. The most accurate portion of this current range, from 50nA to 100μA, should be used for the most critical portion of the desired frequency range.

Consideration of this critical range determines the value of $C_F$, the timing capacitor. The oscillation frequency is given by:

$$f = 3\ I_{EG}/(V_{CC}\ C_F)$$

where $I_{EG}$ is the output current from the exponential generator. If, for instance, the most important frequency range is from 5Hz to 10kHz, then $C_F$ should be 1000pF at $V_{CC}$ = +15V (a low leakage, low tempco capacitor, such as mica, should be used for $C_F$).

Next the reference current for the exponential generator (Current into pin 13 on the 3340, pin 15 on the 3345) is selected. This current ideally should be the geometric mean of the selected generator current range, but consideration of the temperature coefficient of

the bias current for op amp A2 usually dictates a higher value for the reference current. Although this bias current has been temperature compensated, it could have a worst cast tempco of 1000ppm and maximum value of 400nA. Under these conditions, a reference current of 10$\mu$A through $Q_1$, for instance, would have a tempco of 40ppm. It is recommended that, in general, the reference current be selected in the 3$\mu$A to 15$\mu$A range.

Since the reference current pin is a virtual ground summing node, the reference current may be set up with a temperature stable resistor to $V_{CC}$, or other positive stable voltage source. A negative current into this pin will simply gate the exponential generator completely off.

With the value of $C_F$ and reference current now selected, the voltage excursion at the multiplier output, which drives the base of $Q_1$, is now determined for the desired frequency control range. If this range were 1Hz to 20kHz, the exponential generator current, $I_{EG}$, would have to range from 10nA to 200$\mu$A in the above example, requiring the base drive voltage, $V_B$, to vary from +180mV to -78mV, since

$$I_{EG} = I_{REF}\, e^{-V_B/V_T}$$

The most positive voltage at the base of $Q_1$ occurs when the control current, $I_C$, is zero, and is $22V_T\ R_S/R_T$. Therefore, in the above example, $R_T = 22V_T \cdot 1.8K/.18V = 5.72K$, and $R_Z = 3.0R_T/22V_T = 30K$ nominal. Finally, since the multiplier output current must range from +100$\mu$A to -43$\mu$A to produce this desired voltage excursion at the multiplier output and on the base of $Q_1$, the control input current, $I_C$, ranges from 0 to 143$\mu$A. A resistor from $V_{CC}$ to the control input pin may be used to set the oscillator frequency at some initial value with no control voltages applied.

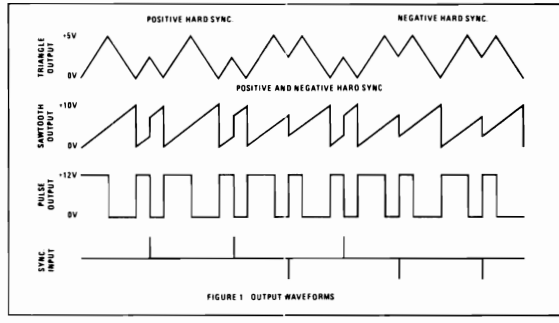


FIGURE 1 OUTPUT WAVEFORMS

The frequency control scale is determined by the value of the input resistor to the control pin, the value of the $Q_1$ base resistor, $R_S$, and the multiplier current gain. Since the multiplier current gain, set by the ratio of the pin 2 current to pin 1 current, should be near unity and $R_S$ should be 1.8K, the control input resistor is the component which should be selected for the desired control scale. For the industry standard scale of 1 octave/volt, the input summing resistors become 100k. The recommended method for trimming the control scale is to tweek the multiplier current gain by adjusting the value of $R_Z$ ±20% about the nominal value.

Both the multiplier and the exponential generator are compensated with the 470$\Omega$ - .01$\mu$F networks shown in the Block Diagrams and are therefore necessary in any application. Since the bandwidth of the multiplier extends beyond the audio range, it may be desirable to limit the bandwidth to reduce possible noise at the base of $Q_1$, thereby reducing FM noise and frequency jitter. This is best accomplished by bypassing $R_S$ to ground with a capacitor, where the corner rolloff frequency is given by: $f_{LP} = 1/(2\pi R_S C)$.

## Trimming The Scale Error

There are two basic sources producing exponential conformity error in the control scale: One is the exponential current generator and the other is the precision multiplier.

The error from the exponential converter is due partly to the bulk emitter resistance of $Q_2$, becoming significant at generator currents greater than 100$\mu$A, and partly to the comparator switching delay, becoming significant at frequencies greater than 5KHz. These two effects cause the oscillator frequency to go flat, but only at the uppermost octaves.

Circuitry has been provided to correct for these effects. The output of the hi-frequency track pin (pin 7 on the 3340, pin 8 on the 3345) is a current which is one fourth the generator output current, $I_{EG}$. This current may be converted with a grounded resistor to a voltage, a portion of which is

then fed back to the control input pin. As the frequency is increased, this feedback voltage will tend to sharpen the control scale, but only at the upper end, since the feedback voltage becomes significant only at the higher generator currents. The amount of voltage fed back is adjusted so the scale is sharpened just enough to compensate for the inherent high end flatness

The method recommended for trimming the control scale is as follows: The hi-frequency track adjust is first set so that no correction voltage is fed to the control input. The oscillator frequency is set around 200Hz and the scale adjust trimmer is adjusted for the desired scale factor (e.g. 1.000 octave/volt). Then the oscillator frequency is set to around 10KHz, and the hi-frequency track trimmer is adjusted for the same scale factor.

The source of error from the precision multiplier is due to the multiplier's gain (nominally unity) changing as the control input current changes. This type of error causes the frequency to become increasingly sharp or flat as the control current is increased. The percentage difference in multiplier gains, and hence scale factors, at any two inputs to the multiplier may be calculated as the percentage error given in the specifications times the difference in $\mu$A between the two corresponding outputs. For example, suppose the scale were adjusted for precisely 1 octave/volt at midrange. At one octave above this adjusted octave, with the multiplier output 10$\mu$A different, the scale factor could be .08% different worst case. This would produce a volts/octave error at the base of $Q_1$ of .08% x 18mV = 14.4$\mu$V, which would cause this octave to be .06% (1 cent) sharp or flat. At five octaves above the adjusted octave, the scale factor could be 0.4% different worst case, producing a volts/octave error of 0.4% x 18mV = 72$\mu$V. This fifth octave would thus be 0.28% (5 cents) sharp or flat. Note that if octaves above the adjusted octaves were sharp, those octaves below the adjusted octave would become increasingly flat, and vice versa.

Typically the error produced by the multiplier is much less than the above example. However, if maintaining a tighter tolerance is required for the particular application, the multiplier error may be trimmed out for each device. The trimming procedure requires that both $R_Z$ and $R_S$ be made adjustable ±30% about the nominal value; $R_Z$ is first adjusted so that the multiplier gain is constant over the selected input current range; then $R_S$ is adjusted for the desired scale factor (adjusting $R_S$ will reintroduce some error, so $R_Z$ may have to be readjusted).

Should for some reason it be desired not to use the temperature compensation circuitry, the multiplier/tempco generator may be bypassed simply by leaving pin 1, pin 2, and the control input pin open, and applying the control voltage to the base of $Q_1$ via the multiplier output pin.

## Waveform Outputs

All waveform outputs are short-circuit protected and may be shorted continuously to any supply without damaging the device. Each output, however, has differing drive capabilities.

Although the triangle output can sink at least .4mA and source over several mA, care must be exercised in loading this output. Because the output has a finite impedance and drives the comparator, a change in load will change the frequency of the oscillator. Adding a 100K resistor to ground, for instance,

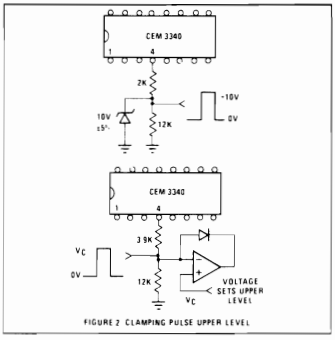


FIGURE 2 CLAMPING PULSE UPPER LEVEL

could lower the frequency by 150/100K = 0.15% (2.5 cents) worst case. A load capacitance will act like a resistor with a value $1/(2fC_L)$ and requires the same considerations as above. A continuous load no greater than 10K and/or 1000pF to ground is recommended.

Since the sawtooth output is buffer isolated from the oscillator circuitry, it can sink at least .6mA and source over several mA with no effect on oscillator performance, and only negligible effect on sawtooth waveshape. Stray capacitance at this output greater than 40pF, however, will cause a small high frequency oscillation. A 100Ω resistor between the output and load is all that is required to isolate more than .01$\mu$F.

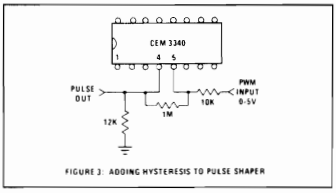


FIGURE 3: ADDING HYSTERESIS TO PULSE SHAPER

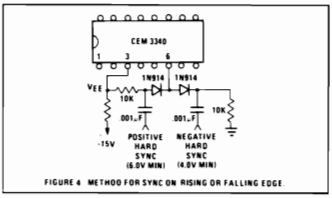


FIGURE 4. METHOD FOR SYNC ON RISING OR FALLING EDGE

The pulse output is an open NPN emitter, and therefore requires a pull-down resistor to ground or to any negative voltage. Any pull-down voltage between ground and .5 volt above the voltage on the negative supply pin will precisely determine the lower level of the pulse wave. For pull-down voltages more negative than this, the lower level will be nearly the negative supply pin voltage. The nominal upper level of the pulse wave is given by: $V_{CC}$ - 0.3V -1.3K · $I_{PLD}$ for $I_{PLD} >$ 0.6mA, and $V_{CC}$ - 0.9V for $I_{PLD} <$ 0.6mA, where $I_{PLD}$ is the pull down current. A maximum value of 3mA for $I_{PLD}$ is recommended. For those applications which require a more stable, well defined upper level, the circuits shown in Figure 2 may be used.

The pulse width of the pulse output may be set from 0 to 100% with a 0 to +5V external voltage ($V_{CC}$ = +15V) applied to the PWM control input pin (pin 5 on the 3340 and 3345). The fall time of the pulse wave is slower than the rise time due to finite comparator gain. It may be speeded up considerably by adding hysteresis as shown in Figure 3. Care should be exercised in the layout to prevent stray capacitive coupling between the pulse output and the PWM input,as this can cause comparator oscillation.

The square wave output (pin 7) from the CEM 3345 also requires a pull down resistor to any negative supply greater than -4 volts. It provides an output swing from nominally 1.3 volts below the hard sync reference voltage to a level nominally the same as the hard sync reference voltage. The Block Diagram shows a convenient way of generating a full swing square wave from this output. The current pulled down from this output should also be limited to a maximum of 3mA.

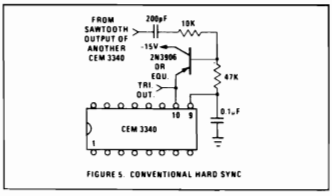


FIGURE 5. CONVENTIONAL HARD SYNC

## Frequency Synchronization

The oscillator frequency may be hard synchronized in several different ways. One way is to couple positive pulses, negative pulses, or both, into the hard sync input pin (pin 6 on the 3340 and 3345). A positive sync pulse will cause the triangle wave to reverse directions only during the rising portion of the triangle, while a negative sync pulse will cause direction reversal only during the falling portion. The resulting waveforms are shown in Figure 1, and provide a wider variety of synchronized sounds than possible through conventionally synchronized oscillators. Simple capacitive coupling as shown in the Block Diagrams allows hard synchronization on both the rising and falling edge of a rectangle wave. Figure 4 shows circuitry for allowing only one or the other of the edges to synchronize the oscillator. The peak amplitude of the pulses actually appearing on the sync pin should be restricted to 1 volt minimum and 3 volts maximum for best operation.

Another method of hard synchronizing the oscillator is shown in Figure 5. Negative pulses only are coupled into the base of the PNP transistor, with a peak amplitude of 8 to 10 volts for best results at $V_{CC}$ = +15V. This method will produce the same waveforms generated by the conventionally synchronized sawtooth oscillators.

Finally, the oscillator may be soft synchronized by negative pulses applied to the threshold voltage pin (pin 9 on the 3340, pin 10 on the 3345). These pulses cause the triangle upper peak to reverse direction prematurely, causing the oscillation period to be an integral multiple of the pulse period. The peak amplitude of these negative pulses should be limited to 5 volts maximum and positive pulses should be avoided entirely. If this input is not used for synchronization purposes, it is recommended that it be bypassed with a 0.1μF capacitor to ground to prevent synchronization or jitter to noise pulses on the $V_{CC}$ supply line.

## Linear FM

The reference current input pin may be used for linear modulation of the frequency. The external input is summed with the reference current simply through a resistor terminating at this pin. For audio FM, it is recommended that a coupling capacitor be used to prevent frequency shift when connecting to the external source. The value of the input resistor should be selected so that the maximum peak to peak input signal produces a plus and minus current equal to the reference current.

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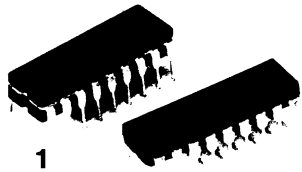
# CEM 3320

## Voltage Controlled Filter

The CEM 3320 is a high performance voltage controlled four-pole filter complete with on-chip voltage controllable resonance. The four independent sections may be interconnected to provide a wide variety of filter responses, such as low pass, high pass, band pass and all pass. A single input exponentially controls the frequency over greater than a ten octave range with little control voltage feedthrough. Another input controls the resonance in a modified linear manner from zero to low distortion oscillation. For those demanding applications, provision has been made to allow trimming for improved control voltage rejection. Each filter section features a novel variable gain cell which, unlike the traditional cell, is fully temperature compensated, exhibits a better signal-to-noise ratio and generates its low distortion predominantly in the second harmonic. The device further includes a minus two volt regulator to ensure low power dissipation and consequent low warm-up drift even with ±15 volt supplies.

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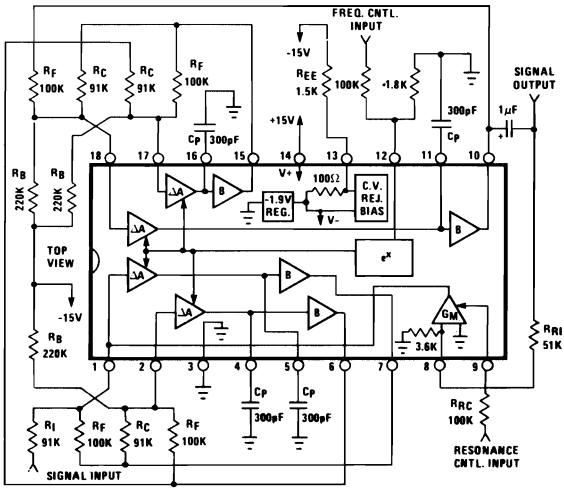
### Circuit Block and Connection Diagram




### Features

- Low Cost
- Voltage Controllable Frequency: 12 octave range minimum
- Voltage Controllable Resonance: From zero to oscillation
- Accurate Exponential Frequency Scale
- Accurate Linear Resonance Scale
- Low Control Voltage Feedthrough: -45dB typical
- Filter Configurable into Low Pass, High Pass, All Pass, etc.
- Large Output: 12V.P.P. typical
- Low Noise: -86dB typical
- Low Distortion in Passband: 0.1% typical
- Low Warm Up Drift
- Configurable into Low Distortion Voltage Controlled Sine Wave Oscillator
- ±15 Volt Supplies

# CEM 3320

## Electrical Characteristics

| $V_{CC}$ = +15V | $R_F$ = 100K | | $T_A$ = 25°C | |
|---|---|---|---|---|
| Parameter | Min. | Typ. | Max. | Units |
| Pole Frequency Control Range | 3500:1 | 10,000:1 | – | |
| Sensitivity of Pole Frequency Control Scale, Midrange | 57.5 | 60 | 62.5 | mV/decade |
| Tempco of Pole Frequency Control Scale | 3000 | 3300 | 3600 | ppm |
| Exponential Error of Pole Frequency Control Scale[1] | – | 4 | 12 | % |
| Gain of Variable Gain Cell at $V_C$=0 | 0.7 | 0.9 | 1.3 | |
| Max Gain of Variable Gain Cell | 2.4 | 3.0 | 3.6 | |
| Tempco of Variable Gain Cell[2] | – | 500 | 1500 | ppm |
| Output Impedance of Gain Cell[2] | 0.5 | 1.0 | 2.0 | MΩ |
| Pole Frequency Control Feedthrough | – | 60 | 200 | mV |
| Pole Frequency Warm-up Drift | – | .5 | 1.5 | % |
| Gm of Resonance Control Element at $I_{CR}$=100uA | .8 | 1.0 | 1.2 | mmhos |
| Amount of Resonance Obtainable Before Oscillation | 20 | 30 | – | dB |
| Resonance Control Feedthrough[3] | – | 0.2 | 1.5 | V |
| Output Swing At Clipping | 10 | 12 | 14 | V.P.P. |
| Output Noise re Max Output[4] | -76 | -86 | – | dB |
| Rejection in Bandreject | 73 | 83 | – | dB |
| Distortion in Passband[5,7] | – | 0.1 | 0.3 | % |
| Distortion in Bandreject[6,7] | – | 0.3 | 1 | % |
| Distortion of Sine Wave Oscillation[8] | – | 0.5 | 1.5 | % |
| Internal Reference Current, $I_{REF}$ | 45 | 63 | 85 | μA |
| Input Bias Current of Frequency Control Input | 0.2 | 0.5 | 1.5 | μA |
| Input Impedance to Resonance Signal Input | 2.7 | 3.6 | 4.5 | KΩ |
| Buffer Slew Rate | 1.5 | 3.0 | – | V/uS |
| Buffer Input Bias Current ($I_{EE}$=8mA) | ±8 | ±30 | ±100 | μA |
| Buffer Sink Capability | .4 | .5 | .63 | mA |
| Buffer Output Impedance[2] | 75 | 100 | 200 | Ω |
| Positive Supply Range | +9 | – | +18 | V |
| Negative Supply Range[9] | -4 | – | -18 | V |
| Positive Supply Current | 3.8 | 5 | 6.5 | mA |

**Note 1:** -25mV < $V_C$ < +155mV. Most of this error occurs in upper two octaves.
**Note 2:** $V_C$ = 0
**Note 3:** Untrimmed. 0 < $I_{CR}$ < 100μA
**Note 4:** Filter is connected as low pass and set for 20 KHz cut-off frequency.
**Note 5:** Output signal is 3dB below clipping point.
**Note 6:** Output signal is 3dB below passband level, which is 3dB below clipping point. In general, this is worst case condition.
**Note 7:** Distortion is predominantly second harmonic.
**Note 8:** Sinewave is not clipped by first stage.
**Note 9:** Current limiting resistor always required.

## Application Hints

### Supplies

In order to minimize the power dissipation, the negative supply is regulated at -1.9 volts with an internal shunt regulator. This not only reduces warm-up drift of the pole frequencies at power turn-on, but also allows virtually any negative supply greater than -4 volts to be used. The current limiting resistor, $R_{EE}$, must always be included and is calculated as follows:

$$R_{EE} = \frac{V_{EE} - 2.7V}{0.008}$$

As can be seen from the Block Diagram, an internal 100Ω resistor is in series between the regulator and pin 13. This resistor, which allows for trimming of the control voltage feedthrough (explained in further detail below) results in an actual voltage at pin 13 of around -2.7 volts.

Although the circuit was designed for a positive supply of +15 volts, any voltage between +9 and +18 volts may be applied to pin 14. The only effect, other than power dissipation, is the maximum possible peak-to-peak output swing in accordance with:

$$V_{OUT}\ (V.P.P.) = V_{CC} - 3V$$

### Operation of Each Filter Stage

Each filter stage consists of a variable gain cell followed by a high input impedance buffer. The variable gain cell is a current-in, current-out device (as opposed to the traditional voltage-in, current-out device) whose output current, $I_{OUT}$, is given by the following expression:

$$I_{OUT} = (I_{REF} - I_{IN})\, A_{IO}\, e^{-V_C/V_T}$$

where $V_T$ = KT/q, $V_C$ is the

## Absolute Maximum Ratings

| | |
|---|---|
| Voltage Between $V_{CC}$ and $V_{EE}$ Pins | +22V,-0.5V |
| Voltage Between $V_{CC}$ and Ground Pins | +18V,-0.5V |
| Voltage Between $V_{EE}$ and Ground Pins | -4V,+0.5V |
| Voltage Between Cell Input and Ground Pins | +0.5V,-6V |
| Voltage Between Frequency Control and Ground Pins | ±6V, |
| Voltage Between Resonance Control and Ground Pins | +2V,-18V |
| Current Through Any Pin | ±40mA |
| Storage Temperature Range | -55°C to +150°C |
| Operating Temperature Range | -25°C to +75°C |

voltage applied to pin 12, $A_{IO}$ is the current gain of the cell at $V_C$ = 0 (Nominally 0.9), and

$$I_{REF} = \frac{.46V_{CC} - .65V}{100K^*}$$

*±25%

As the input to the variable cell is a forward biased diode to ground, it presents essentially a low impedance summing node at a nominal 650mV above ground. The required input currents may therefore be obtained with resistors terminating at this input node.

For normal operation of any filter type, each stage is set up with a feedback resistor, $R_F$, from the buffer output to the variable gain cell input, and with the pole capacitor, $C_P$, connected to the output of the variable gain cell. This setup is shown in Figure 1. In the D.C. quiescent state, the buffer output will always adjust itself so that a current equal to $I_{REF}$ flows into the input.

For lowest control voltage feedthrough and maximum peak-to-peak output signal, the quiescent output voltage of each buffer, $V_{ODC}$, should be:

$$V_{ODC} = .46V_{CC}$$

Thus, in the simple case of Figure 1, $R_F$ is calculated as follows:

$$R_F = \frac{V_{ODC} - .65V}{I_{REF}}$$

$$= 100K \text{ nominal}$$

Since $I_{REF}$ can vary ±25%, $V_{ODC}$ can vary nearly 30% from device to device using a standard 5% resistor for $R_F$. In the typical case where $V_{CC}$ = +15V, $I_{REF}$ is 63μA nominal, and the D.C. output of each buffer should be set for +6.9V nominal.

The output impedance of the variable gain cell, although high, has a finite value. This impedance is reflected back to the input as an A.C. resistance of nominally 1 megohm in parallel with the feedback resistor, $R_F$, regardless of control voltage value. The pole frequency of each filter section is determined by the total equivalent feedback resistance, $R_{EQ}$, and the pole capacitor in the expression:

$$f_P = \frac{A_{IO}}{2\pi R_{EQ} C_P} e^{-V_C/V_T}$$

where:

$$R_{EQ} = \frac{R_F \cdot 1M\Omega^*}{R_F + 1\,M\Omega^*}$$

*-50%, +100%

### Signal Coupling into a Filter Section

For the filter section to provide the low pass function, the input signal is coupled via a scaling resistor, $R_C$, into the input. If the signal is the external input to the entire filter, it will in general have a D.C. quiescent voltage level of zero, and all of $I_{IN}$ equal to $I_{REF}$ for the first stage will be provided by its feedback resistor. If the signal is from the output of a previous filter section, it will have a quiescent level of $.46V_{CC}$ (6.9 volts for a +15 volt supply). Therefore, part of $I_{IN}$ will be supplied by this voltage through $R_C$ while the remainder will be sourced through $R_F$.

The voltage gain in the passband is given by $R_{EQ}/R_C$. In general, this gain should be set to unity for stages two, three and four. The input resistor to stage one can be scaled for any size of the external input signal. The resistance value should be selected so that the maximum external input signal produces the maximum passband output signal before clipping.

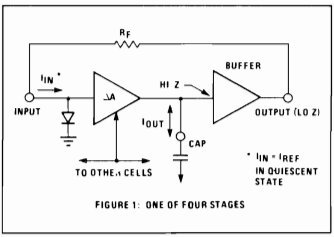


FIGURE 1: ONE OF FOUR STAGES

To generate the hi-pass function, the input signal is coupled into the variable gain element output via the pole capacitor, $C_P$. Therefore, any D.C. voltage level is blocked by the capacitor and $I_{IN}$ equal to $I_{REF}$ for each input is supplied only through the feedback resistors. The voltage gain in the pass band is simply unity, regardless of the value of $R_F$. For best results, the output impedance of whatever is generating the external input signal to stage one should be low compared to $R_F/4$.

## Sample Filter Circuits

The Block Diagram shows the external components connections for a four-pole, low-pass filter designed to operate off ±15 volt supplies. The values for $R_F$, $R_C$, and $R_B$ were chosen so that a) when the 1 megohm reflected resistance is in parallel with $R_F$, the gain of stages two, three and four is unity, and b) with the buffer outputs at the proper quiescent level of 6.9 volts, the total current into each input is the required 63$\mu$A. For stage 1, all of this quiescent current is sourced by the feedback resistor. For stages two, three, and four, 63$\mu$A is sourced by the feedback resistor, while 70$\mu$A is sourced by the coupling resistor for a total sourced current of 133$\mu$A. Thus, to end up with a net quiescent input current of 63$\mu$A, 70$\mu$A is sunk out of the input by bias resistor, $R_B$.

If connecting the filter input to an external signal causes the D.C. level of the filter output to change more than several volts, it is recommended that an input coupling capacitor be used such as shown in Figure 4.

Figures 2, 3, 4, and 5 show high-pass, band-pass, all-pass, and state variable realizations, all with the voltage controlled resonance feature. Note that due to the configuration of the resonance feedback, the resonance frequency of the high-pass will be approximately 2.4 times higher than that of the low-pass, while the resonance frequency of the band-pass and all-pass will be 1/2.4 = .42 times lower than that of the low-pass, for the same component values. For the state variable, resistor $R_Q$ adds positive feedback to increase the maximum Q, which is otherwise limited by the reflected 1MΩ impedance across the integrators.

## Pole Frequency Control Scale

The current gains of each of the four sections (and consequently their pole frequencies) are controlled simultaneously with a voltage applied to pin 12. Since the scale is exponential with the standard 18mV/octave (60mV/decade), an input attenuator network will in most cases be required. An increasing positive control voltage lowers the pole frequencies of the filter. For best results over a thousand-to-one control range, the voltage on pin 12 should be maintained between -25mV and +155mV.

Unlike the typical variable transconductance cell used in most V.C. filters, the four stages in the CEM 3320 are fully temperature compensated. The only remaining first order temperature effect is that of control scale sensitivity ($1/V_T$). This effect may be compensated in the usual manner with a +3300ppm tempco resistor (Tel Labs Q81).

## Resonance Control

The variable gain cell used to control the amount of resonance is the traditional transconductance type of amplifier. It has a separate signal voltage input

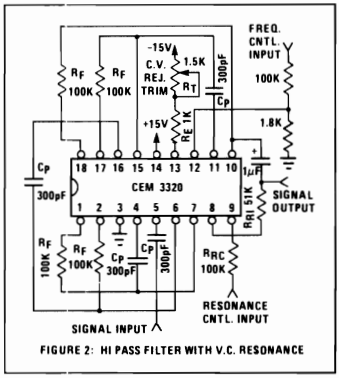



FIGURE 2: HI PASS FILTER WITH V.C. RESONANCE

(pin 8), a separate control current input with a modified linear scale (pin 9), and a current output internally connected to the input of stage one. With an impedance of 3.6K ±900Ω, the input is referenced to ground; thus, connection to the filter output will require a coupling capacitor.

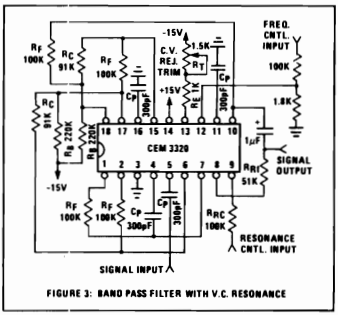



FIGURE 3: BAND PASS FILTER WITH V.C. RESONANCE

Control of the transconductance is accomplished with a current input. As the control input is a low impedance summing node at a potential near ground, the control current may be derived from the resonance control voltage with an input resistor, $R_{RC}$, terminated at pin 9. This resistor should be selected so that the maximum available resonance control voltage produces the maximum desired control current.

Figure 6 shows a graph of the transconductance versus control current. As can be seen, the slope of the curve becomes more gradual as the control current increases. This feature allows the resonance to be controlled with finer resolution as the critical point of oscillation is approached.

The maximum control current is therefore selected in accordance with the amount of control sensitivity which is desired at the top of the control range. The value of the input resistor, $R_{RI}$, is then selected depending on where in the control scale oscillation is desired to begin (when the control voltage is 90% of the maximum value, for instance). The following formula may be used:

$$R_{RI} = 3.6K^{*} \left(\frac{Gm_{OSC}\, R_{EQ} - 1}{A_{OSC}}\right)$$

*±25%

where $Gm_{OSC}$ is the transconductance corresponding to the control current at which oscillation is desired to begin; and where $A_{OSC}$ is the overall gain from the resonance signal input resistor, $R_{RI}$, to the filter output required to sustain oscillation. If the gain of stages 2, 3 and 4 are unity, then $A_{OSC}$ = 12dB or 4 in the case of the low pass filter.

While operating the filter in the resonant mode, care should be taken not to overload the input to the filter. If the signal output of stage one is allowed to become clipped, then not only will the apparent resonance of the signal at the filter output appear to be reduced, but the D.C. level of the output signal will shift.

When the resonance control is advanced until sustained oscillations are produced, advancing the resonance control further will merely increase the amplitude of the oscillation. A lesser effect is the shift of the oscillation frequency. For minimum shift (typically less than 0.5%), the oscillation amplitude should be kept below the clipping level of the first stage output. Allowing the oscillation to be clipped will produce frequency shifts in excess of 5%.

## Other Uses of the Resonance Control Cell

Other than controlling the resonance, the variable transconductance amplifier may be used as an independent VCA controlling the amplitude of the input signal to the filter. Or the cell may be set up as a symmetrical limiter/clipper for either preventing large dynamic input signals from overloading the filter or for providing additional coloration to the input signal.

## Pole Frequency Control Voltage Rejection

The D.C. voltage shift at the filter output due to the frequency control voltage may be minimized by adjusting the current into the minus supply pin, pin 13. This is accomplished by replacing the negative supply current limiting resistor, $R_{EE}$,

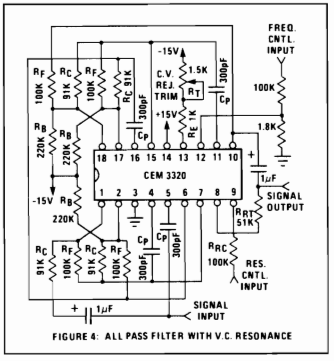


FIGURE 4: ALL PASS FILTER WITH V.C. RESONANCE

with a series resistor and trim pot. The fixed resistor, $R_E$, and series trim pot, $R_T$, should be selected so that the current into pin 13 may be adjusted from 5mA to 12mA. Or:

$$R_E = \frac{V_{EE} - 3.2V}{12mA}$$

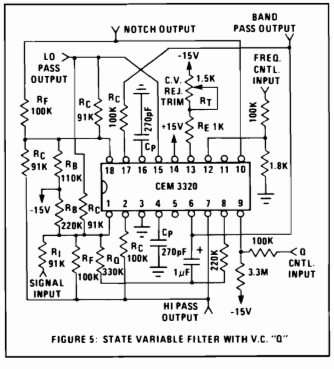


FIGURE 5: STATE VARIABLE FILTER WITH V.C. "Q"

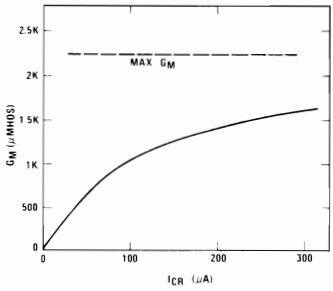



FIGURE 6: TRANSCONDUCTANCE V.S. CONTROL CURRENT OF RESONANCE CELL

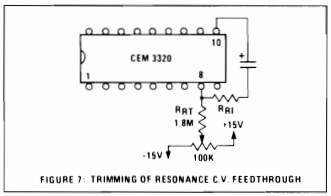



FIGURE 7: TRIMMING OF RESONANCE C.V. FEEDTHROUGH

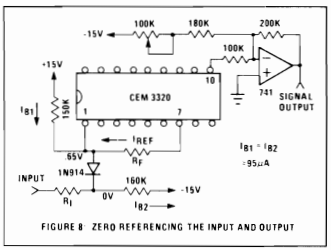



FIGURE 8: ZERO REFERENCING THE INPUT AND OUTPUT

and

$$R_T \approx \frac{V_{EE} - 2.4V}{5mA} - R_E$$

These components are shown in the filter circuits of Figures 2-5. To obtain minimum control voltage feedthrough, the best technique for adjusting this trim is to switch back and forth between the maximum and minimum control voltages while adjusting the pot so that the D.C. output voltage at these two extreme conditions is the same.

## Resonance Control Voltage Rejection

For most applications, no trimming should be necessary. However, if required, the resonance control voltage feed through may be minimized by applying a small D.C. voltage on the resonance signal input pin, pin 8. A typical set-up is shown in Figure 7. The value of $R_{RT}$ should be selected so the trim pot is able to adjust the voltage on pin 8 by ± 30mV.

## Stage Buffers

Each buffer can source up to 10mA and sink a nominal 500μA. However, any D.C. load greater than ±200μA to ±300μA may begin to degrade the performance of the filter, especially if the loads on each buffer differ by more than this amount. The maximum recommended D.C. loads are 1mA source, 250μA sink, and a 150μA load difference between buffers. The maximum recommended A.C. loads are ±250μA.

Since the D.C. level at the filter output is at some non-zero voltage (6.9 volts for $V_{CC}$ = +15V), a coupling capacitor will be required somewhere in the signal chain, either at the filter output or the following device inputs. Note that if the resonance feature is being used, the filter output is already D.C. blocked by the resonance input coupling capacitor, thus providing a convenient output point. If D.C. coupling to ground referenced inputs and outputs is required, the schemes shown in Figure 8 may be used. Note that the output circuit has the benefits of 1) allowing for gain after the filter, and 2) providing an output with greater drive capability. The buffer outputs are not short circuit protected; therefore care should be exercised to not short the outputs to ground or either supply.

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# The Blacksburg Group

According to Business Week magazine (Technology July 6, 1976) large scale integrated circuits or LSI "chips" are creating a second industrial revolution that will quickly involve us all. The speed of the developments in this area is breathtaking and it becomes more and more difficult to keep up with the rapid advances that are being made. It is also becoming difficult for newcomers to "get on board."

It has been our objective, as The Blacksburg Group, to develop timely and effective educational materials that will permit students, engineers, scientists, technicians and others to quickly learn how to use new technologies and electronic techniques. We continue to do this through several means, textbooks, short courses, seminars and through the development of special electronic devices and training aids.

Our group members make their home in Blacksburg, found in the Appalachian Mountains of southwestern Virginia. While we didn't actively start our group collaboration until the Spring of 1974, members of our group have been involved in digital electronics, minicomputers and microcomputers for some time.

Some of our past experiences and on-going efforts include the following:

–The design and development of what is considered to be the first popular hobbyist computer. The Mark-8 was featured in Radio-Electronics magazine in 1974. We have also designed several 8080-based computers, including the MMD-1 system. Our most recent computer is an 8085-based computer for educational use, and for use in small controllers.

–The Blacksburg Continuing Education Series™ covers subjects ranging from basic electronics through microcomputers, operational amplifiers, and active filters. Test experiments and examples have been provided in each book. We are strong believers in the use of detailed experiments and examples to reinforce basic concepts. This series originally started as our Bugbook series and many titles are now being translated into Chinese, Japanese, German and Italian.

–We have pioneered the use of small, self-contained computers in hands-on courses for microcomputer users. Many of our designs have evolved into commercial products that are marketed by E&L Instruments and PACCOM, and are available from Group Technology, Ltd., Check, VA 24072.

–Our short courses and seminar programs have been presented throughout the world. Programs are offered by The Blacksburg Group, and by the Virginia Polytechnic Institute Extension Division. Each series of courses provides hands-on experience with real computers and electronic devices. Courses and seminars are provided on a regular basis, and are also provided for groups, companies and schools at a site of their choosing. We are strong believers in practical laboratory exercises, so much time is spent working with electronic equipment, computers and circuits.

Additional information may be obtained from Dr. Chris Titus, the Blacksburg Group, Inc. (703) 951-9030 or from Dr. Linda Leffel, Virginia Tech Continuing Education Center (703) 961-5241.

Our group members are Mr. David G. Larsen, who is on the faculty of the Department of Chemistry at Virginia Tech, and Drs. Jon Titus and Chris Titus who work full-time with The Blacksburg Group, all of Blacksburg, VA.

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